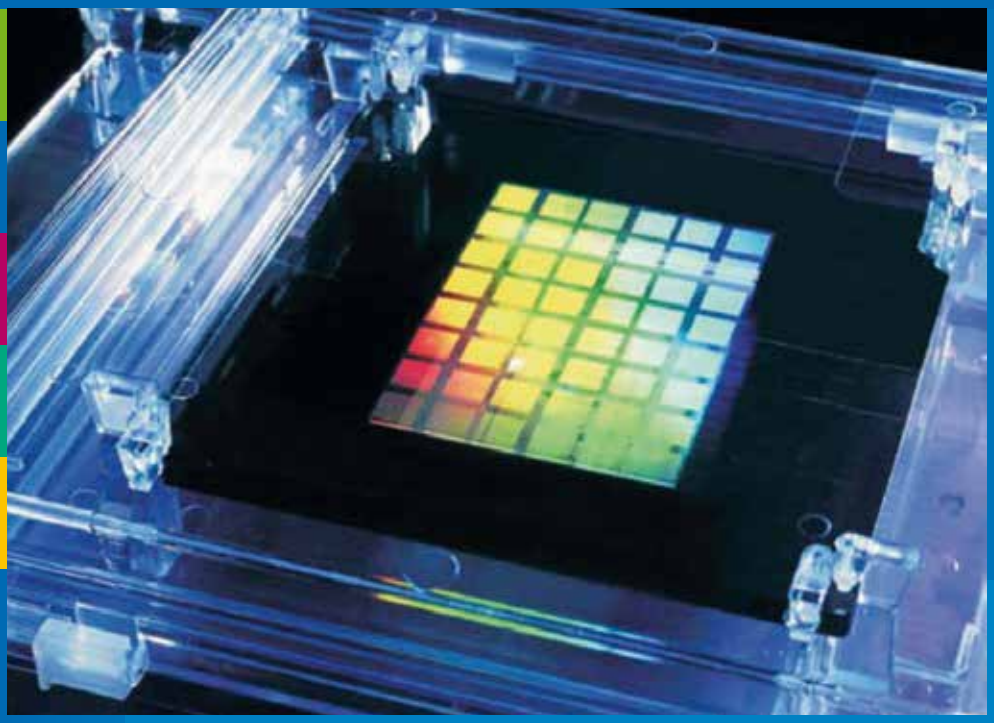
PROGRAM & ABSTRACTS



# THE 34th EUROPEAN MASK AND LITHOGRAPHY CONFERENCE

# EMLC 2018

June 18 – 20, 2018
MINATEC Conference Center, Grenoble, France

www.emlc-conference.com

GMM VDI VDE

# 34th European Mask and Lithography Conference
# EMLC 2018
# at the MINATEC Conference Center, Grenoble, France
# on Monday, June 18th to Wednesday, June 20th 2018

## Welcome to the EMLC 2018 in Grenoble

On behalf of VDE/VDI-GMM, the EMLC 2018 Sponsors, and the EMLC 2018 Organizing Committee, we would like to welcome you to the 34th European Mask and Lithography Conference, EMLC 2018, at the MINATEC Conference Centre in the City of Grenoble, France.

The conference has annually brought together scientists, researchers, engineers, and technologists from research institutes and companies from around the world to present innovations at the forefront of mask lithography and mask technology.

The two and a half days conference (starting on Monday June 18th at 02:00 PM in the MINATEC Conference Centre with a Tutorial Session (ending at 05:00 PM). At 5:00 PM a short Welcome Reception and the Poster Session will take place till about 6:00 PM. The Poster Session will continue on Tuesday afternoon.

The Technical Sessions (including the second part of the Poster Session) of the EMLC2018 Conference starts on Tuesday, June 19th from 09:00 AM till 06:45 PM), and on Wednesday, June 20th from 09:00 AM till 06:15 PM.
The EMLC2018 conference is dedicated to the science, technology, engineering and application of mask and lithography technologies and associated processes, giving an overview of the present status in mask and lithography technologies and the future strategy where mask producers and users have the opportunity of becoming acquainted with new developments and results. This year the EMLC2018 Program Committee defined the following sessions:

“Wafer Lithography – 193i and EUV”; “Mask-Less Lithography, Nano-Imprint Lithography, and Directed Self Assembly”; “Mask Patterning, Metrology and Process”; “Non-IC Applications, Plasmonics and Photonics”; “Mask2Wafer and Wafer2Wafer Metrology” ; and “Using Big Data / Deep Learning”.

Of course, papers outside these predefined areas of interest were welcome for submission as well.
As Welcome Speaker from the City of Grenoble Mme Marie-José Salat, representative of Grenoble-Alpes Métropole, will demonstrate the importance of Grenoble as one of the three “High Technology Centres in Europe”. Besides Dresden and Leuven/Eindhoven, Grenoble, Europe’s Smart Valley, offers thousands of jobs in computing & software as well as in Micro-Nanotechnology & Electronics.

Regarding the Tutorial Session on Monday afternoon, we asked Paul van Adrichem, from ASML Netherlands B.V., Veldhoven, Netherlands to give a **“Review of OPC / RET / SMO”**.


This tutorial will provide an overview of advanced Optical Proximity Correction, Resolution Enhancement Technology as well as Source-Mask-Optimization.

As second tutor we asked Aviram Tam, from Applied Materials PDC Israel. He will explain the **"Inspection Challenges in the EUV Area"**.

This tutorial will cover the use cases for blank inspection, pattern inspection, outgoing inspection and the possible solution for DUV mask inspection ,e-Beam MI, Actinic blank inspection, on-wafer qualification and how those evolve in each of the different scenarios for pellicle (no pellicle/detachable/13.5nm only/193nm friendly). The tutor will be from the Mask Inspection Product Group of Applied Materials, Israel.

As first Keynote Speaker we have invited Olivier Noblanc from STMicroelectronics, Crolles, France. He will talk about **"Technology for Optical Sensors"**.

The second Keynote Speaker is Laurent Pain from CEA-LETI, Grenoble, France. His presentation is entitled: **"The Battle Field of Lithography"**.

The third Keynote Speaker is Frédéric Boeuf from STMicroelectronics, Crolles, France. He will present the newest technologies on **"Silicon Photonics: from research to industrial reality"**.

There are several invited talks: on Multi-Beam Mask Writing, on Multi-Trigger Resist for Electron Beam and Extreme Ultraviolet Lithography, on Photonic Superlattice Multilayers for EUV Lithography Infrastructure, on EUV Pellicle Industrialization Progress, on Mask-Less Lithography, on Wafer-Level UV-Nanoimprint Lithography, on Directed Self-Assembly, on Lithography Technology and Trends for More than Moore Devices, on Reticle Critical Dimension Uniformity Improvement, and on Automatic Defect Classification of SEM images using Deep Learning.

As every year, we have invited the authors of the Best Poster of BACUS (SPIE Photomask Technology) 2017 and we will invite the Best Paper from Photo Mask Japan 2018 to present their papers.

**Technical Exhibition**

Parallel to the Conference Presentations, a Technical Exhibition will take place on Monday (5:00 PM to 6:00 PM) continuing on Tuesday (10:00 AM to 06:00 PM) and on Wednesday (10:00 AM to 04:00 PM) where companies (mask suppliers, material suppliers and equipment suppliers) will exhibit their companies and products.

To foster the exchange between the conference attendees and the exhibitors, the exhibition area will also be the place for all coffee and lunch breaks.

**Conference Dinner Banquet**

For Tuesday evening, June 19th, after the Poster Session we have organized the Conference Banquet Dinner at the Bastille", 300 meters above Grenoble with a fantastic view over the City.

So, please enjoy the Tutorial and the Technical Sessions of the EMLC 2018 as well as the Technical Exhibition, but also allow yourself to visit the beautiful city of Grenoble.

*Uwe Behringer*
EMLC 2018 Conference Chair

## The EMLC 2018 International Program Committee

### Conference Chairs

*Behringer, Uwe,* UBC Microelectronics, Ammerbuch, Germany
*Finders, Jo,* ASML, Veldhoven, The Netherlands

### Co-Conference Chairs

*Connolly, Brid,* Toppan Photomasks GmbH, Dresden, Germany
*Gale, Chris,* Applied Materials, Dresden, Germany
*Hayashi, Naoya,* DNP, Saitama, Japan

### Program Chairs

*Stolberg, Ines*, Vistec Electron Beam, Jena, Germany
*Erdmann, Andreas,* Fraunhofer IISB, Erlangen, Germany

### Co-Program Chairs

*Seltmann, Rolf,* Globalfoundries, Dresden, Germany
*Sarlette, Daniel,* Infineon, Dresden, Germany

### Other Members

*Ehrmann, Albrecht*, Carl Zeiss SMT, Oberkochen, Germany
*Farrar, Dave*, Hoya Corporation, London, UK
*Galler, Reinhard*, EQUIcon, Jena, Germany
*Jonckheere, Rik,* IMEC, Leuven, Belgium
*Kapilevich, Izak*, Applied Materials Inc., Santa Clara, CA, USA
*Lauche, Barbara*, Photronics MZD GmbH, Dresden, Germany
*Le Gratiet, Bertrand*, STMicroelectronics, Crolles, France
*Levinson, Harry*, Globalfoundries, Santa Clara, CA, USA
*Loeschner, Hans*, IMS Nanofabrication GmbH, Vienna, Austria
*Muehlberger, Michael*, Profactor GmbH, Steyr-Gleink, Austria
*Pain, Laurent*, CEA-LETI, Grenoble, France
*Peters, Jan Hendrik*, bmbg consult, Radebeul, Germany
*Progler, Chris*, Photronics Inc., San Jose, CA, USA
*Roeth, Klaus-Dieter*, KLA-Tencor MIE, Weilburg, Germany
*Savari, Serap*, Texas A&M University College Station, USA
*Scheruebl, Thomas*, Carl Zeiss SMT GmbH, Jena, Germany
*Schnabel, Ronald*, VDE/VDI-GMM, Frankfurt am Main, Germany
*Schulze, Steffen*, Mentor Graphics Corp., Wilsonville, OR, USA
*Tschinkl, Martin*, AMTC, Dresden, Germany
*Waelpoel, Jacques*, ASML, Veldhoven, The Netherlands
*Wiley, Jim*, ASML US Inc., Santa Clara, CA, USA
*Wolf, Hermann*, Photronics MZD GmbH, Dresden, Germany
*Wurm, Stefan*, ATICE LLC, Albany, NY, USA
*Yoshitake, Shusuke,* NuFlare, Yokohama, Japan
*Zurbrick, Larry*, Keysight Technologies, Santa Clara, CA, USA

**Abstract Page**

## Monday, June 18th, 2018

**14:00-17:00 The EMLC2018 Tutorial Class**

**14:00 Welcome**
*Uwe Behringer, UBC Microelectronics, EMLC2018 Conference Chair*

**Introduction of the 1st Tutorial Speaker**
*Izak Kapilevic, Applied Materials, USA*

**14:05-15:20 Inspection Challenges in the EUV Area**
*Aviram Tam, Applied Materials PDC, Israel*

This Tutorial will cover the use cases for blank inspection, pattern inspection, outgoing inspection, and the possible solution for DUV mask inspection, eBeam MI, Actinic blank inspection, on-wafer qualification, and how those evolve in each of the different scenarios for pellicle (no pellicle / detachable / 13.5 nm only / 193 nm friendly).

**15:20-15:40 Coffee Break**

**15:40-15:45 Introduction of the 2nd Tutorial Speaker**
*Jo Finders, ASML Netherlands B.V., EMLC2018 Conference Chair*

**15:45-17:00 Review of OPC / RET / SMO**
*Paul van Adrichem, ASML Netherlands B.V., Veldhoven, Netherlands*

This tutorial will provide an overview of advanced Optical Proximity Correction, Resolution Enhancement Technology as well as Source-Mask-Optimization.

**17:00 Get-Together and 1st Poster Session**
Uwe Behringer, Chair of EMLC2018, welcomes the participants and invites them to join the Get-Together concurrently with the first Poster Session.

**17:05-18:00**

**1st Part of Poster Presentations**

*Chair: U. Behringer, UBC Microelectronics, Ammerbuch, Germany; Co-Chair: R. Seltmann, GLOBALFOUNDRIES, Dresden, Germany*

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## Tuesday, June 19th, 2018

**09:00 Welcome and introduction**
*U. Behringer, UBC Microelectronics, EMLC2018 Conference Chair*

**09:10 City of Grenoble Welcome**
**Grenoble-Alpes Métropole Welcomes You (Invited)**
*M.-J. Salat, Grenoble-Alpes Métropole, Grenoble, France*

**09:30-10:25**

### Session 1 – 1st Plenary

*Chair: J. Finders, ASML Netherlands B.V., EMLC2018 Conference Chair*
*Co-Chair: J. Wiley, ASML US Inc., Santa Clara, USA*

31 **09:30 Technology for Optical Sensors (Keynote)**
*O. Noblanc, STMicroelectronics, Crolles, France*

32 **10:00 Best Poster of BACUS 2017: Transparent and conductive backside coating of EUV Lithography Masks for ultrashort pulse Laser Correction (Invited)**
*R. A. Maniyara[1], D. S. Ghosh[1], V. Pruneri[1,2]*
*[1] ICFO - Institut de Ciències Fotòniques, The Barcelona Institute of Science and Technology, Barcelona, Spain*
*[2] ICREA - Institució Catalana de Recerca I Estudis Avançats, Barcelona, Spain*

**10:25-10:50 Coffee Break**

**10:50-12:10**

### Session 2 – 2nd Plenary

*Chair: R. Galler, EQUIcon, Jena, Germany*
*Co-Chair: U. Buttgereit, Carl Zeiss SMT, Jena, Germany*

34 **10:50 The Battle Field of Lithography (Keynote)**
*L. Pain, CEA-LETI, Minatec Campus, Genoble, France*

35 **11:20 Multi-Beam Mask Writer – Enabling Tool for EUV Lithography (Invited)**
*P. Mayrhofer, C. Klein, E. Platzgummer, IMS Nanofabrication GmbH, Vienna, Austria*

37 **11:45 Multi-beam mask writer MBM-1000 for advanced mask making (Invited)**
*H. Matsumoto, H. Yamashita, H. Matsumoto, N. Nakayamada, NuFlare Technology, Inc., Yokohama, Kanagawa, Japan*

**12:10-13:20 Lunch Break**

**Abstract Page**

**13:20-15:20**

**Session 3 – Wafer Lithography (193i and EUV)**

*Chair: J. Finders, ASML Netherlands B.V., Veldhoven, Netherlands*
*Co-Chair: S. Wurm, ATICE-LLC, Albany, NY, USA*



**15:20-15:45 Coffee Break**

**Abstract Page**

**15:45-17:40**

## Session 4 – ML2, NIL, and DSA

*Chair: I. Stolberg, Vistec Electron Beam GmbH, Jena, Germany*
*Co-Chair: B. Connolly, TOPPAN Photomask, Dresden, Germany*

**49** **15:45** **Performance Validation of Mapper's FLX-1200 (Invited)**

*J. Pradelles[1], Y. Blancquaert[1], S. Landis[1], L. Pain[1], G. Rademaker[1], I. Servin[1], G. de Boer[2], P. Brandt[2], M. Dansberg[2], R. Jager[2], J. Peijster[2], E. Slot[2], S. Steenbrink[2], M. Wieland[2]*
*[1] CEA-LETI, Grenoble, France*
*[2] MAPPER Lithography, Delft, The Netherlands*

**51** **16:10** **Feasibility of monitoring a multiple e-beam tool using scatterometry and machine learning: CD and stitching error detection**

*G. Rademaker[1,2], Y. Blancquaert[1], T. Labbaye[1], L. Mourier[1], N. Figueiro[3], F. Sanchez[3], R. Koret[4], J. Pradelles[1], S. Landis[1], S. Rey[1], R. Haupt[3], B. Bringoltz[4], M. Shifrin[4], D. Kandel[4], A. Ger[4], M. Sendelbach[5], S. Wolfling[4], L. Pain[1]*
*[1] CEA-LETI, Minatec Campus, Grenoble, France*
*[2] University Grenoble Alpes, Grenoble, France*
*[3] Nova Measuring Instruments GmbH, Dresden, Germany*
*[4] Nova Measuring Instruments, LTD, Rehovot, Israel*
*[5] Nova Measuring Instruments, Inc., Santa Clara, California, USA*

**53** **16:30** **Wafer-Level UV-Nanoimprint Lithography for high resolution and complex 3D Structures (Invited)**

*T. Glinsner[1], M. Eibelhuber[1], G. Berger[1], M. Chouiki[1], C. Lenk[2], M. Hofmann[2], S. Lenk[2], T. Ivanov[2], I. W. Rangelow[2], A. Ahmad[3], A. Reum[3], M. Holz[3]*
*[1] EV Group, St. Florian am Inn, Austria*
*[2] TU Ilmenau, Germany*
*[3] Nanoanalytik GmbH, Imenau, Germany*

**Abstract Page**

**55** **16:55** **Application of rules-based corrections for wafer scale nanoimprint processes and evaluation of predictive models**
*H. Teyssedre[1], P. Quemere[1], J. Chartoire[1], F. Delachat[1,2], F. Boudaa[1], L. Perraud[1], M. May[1]*
*[1] CEA-LETI, Minatec Campus, Grenoble, France*
*[2] INTITEK, Lyon, France*

**58** **17:15** **Silicon nanowires patterning using UV-assisted graphoepitaxy DSA lithography (Invited)**
*M. Argoud[1], G. Claveau[1], P. Pimenta Barros[1], Z. Chalupa[1], G. Chamiot-Maitral[1], C. Navarro[2], C. Nicolet[2], I. Cayrefourcq[3], R. Tiron[1]*
*[1] CEA-LETI, Minatec Campus, Grenoble, France*
*[2] ARKEMA FRANCE, Lacq, France*
*[3] ARKEMA FRANCE, Colombes, France*

**17:45-18:45**

**Session 5 – 2nd Part of Poster Presentations**

*Chair: U. Behringer, UBC Microelectronics, Ammerbuch, Germany*
*Co-Chair: R. Seltmann, GLOBALFOUNDRIES, Dresden, Germany*

**Poster: Wafer Lithography – 193i and EUV**

**62** **P1** **Alternative absorber materials for mitigation of mask 3D effects in high NA EUV lithography**
*F.J. Timmermans, J. Finders, J. Mcnamara, E. van Setten, ASML Netherlands B.V., Veldhoven, Netherlands*

**65** **P2** **Advances in multi-layer deposition of EUV mask blanks: Current status and roadmap**
*K. Rook, S. Kohli, M. Lee, B. Druz, F. Cerio, A. Devasahayam, Veeco, Plainview, NY, USA*

**67** **P3** **Revival of grayscale technique in power semiconductor processing under low-cost manufacturing constraints**
*J. Schneider, D. Kaiser, N. Morgana, H. Feick, Infineon Technologies Dresden GmbH, Dresden, Germany*

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**Poster: ML2, Nano-Imprint Lithography and DSA**



**Poster: Mask Patterning, Metrology and Process**

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**Abstract Page**

## Poster: Mask2Wafer and Wafer2Wafer Metrology



## Poster: Using Big Data / Deep Learning



**18:45 Street car or walk to the Cable Car Ground Station**
The walking distance from MINATEC Conference Center to the Cable Car Ground Station is about 25 minutes.

**19:30-22:00 Conference Dinner at the "Restaurant le Téléférique" on top of the "Bastille"**
(300 m above Grenoble)

**after 22:00** From Cable Car ground station individual walk or taxi back to your hotel.

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## Wednesday, June 20th, 2018

**09:00-10:00**

**Session 6 – 3rd Plenary**

*Chair: U. Behringer, UBC Microelectronics, Ammerbuch, Germany*

**09:00 Announcements:**

**Uwe Behringer: Best Poster EMLC 2018**

**Jim Wiley: Announcement of SPIE Photomask Technology & EUV Lithography (BACUS) Conference, 17-20 Sept., Monterey, California, USA**

**100** **09:05 Silicon Photonics: from research to industrial reality (Keynote)**
*F. Bœuf, STMicroelectronics, Crolles, France*

**101** **09:35 Lithography technology and trends for More than Moore devices – Advanced Packaging & MEMS devices (Invited)**
*A. Pizzagalli, Yole Développement, Lyon, France*

**10:00 Best Paper of Photomask Japan 2018 (Invited)**
**Title: Development of closed-type EUV pellicle**
*Yosuke Ono, Kazuo Kohmura, Atsushi Okubo, Daiki Taneichi, Hisako Ishikawa, Tsuneaki Biyajima, Mitsui Chemicals Inc., Tokyo, Japan*

**10:25-10:50 Coffee Break**

**Abstract Page**

**10:50-12:30**

**Session 7 – Mask Patterning, Metrology and Process**

*Chair: M. Tschinkl, AMTC, Dresden, Germany*
*Co-Chair: K.-D. Roeth, KLA-Tencor MIE, Weilburg, Germany*

**104** **10:50** **Lithographic solution for yield detracting patterning defect signatures caused by Layout and Unit Process Recipe interaction**
*M. Voigt, R. Gaertner, R. Seltmann, GLOBALFOUNDRIES, Dresden, Germany*

**106** **11:10** **CK-MASK semi-manual tool for mask inspection and blowing**
*A. Leserri, U. Lessi, F. Ferrario, ST Microelectronics, Agrate, Italy*

**109** **11:30** **The (almost) completely automated 12”-lithography**
*J. Seyfert, L. Albinus, J. Arnold, S. Fritsche, S. Habel, M. Mitrach, M. Stephan, Infineon Technologies Dresden GmbH, Dresden, Germany*

**111** **11:50** **Fast local registration measurements for efficient e-beam writer qualification and correction**
*K.-D. Roeth, H. Steigerwald, R. Han, O. Ache, F. Laske, KLA-Tencor MIE GmbH, Weilburg, Germany*

**113** **12:10** **Failure analysis and prevention of patterning issues using OPC simulation and advanced method of contour analysis**
*C. Beylier, F. Robert, B. Vianne, STMicroelectronics, Crolles, France*

**12:30-13:40 Lunch Break**

**Abstract Page**

**13:40-15:00**

**Session 8 – Non-IC Applications, Plasmonics & Photonics**

*Chair: R. Tiron, CEA-LETI, Grenoble, France*
*Co-Chair: T. Onanuga, Fraunhofer IISB, Erlangen, Germany*

**115** **13:40** **Accurate determination of 3D PSF and resist effects in grayscale laser lithography**

*T. Onanuga[1,2,3], C. Kaspar[4], H. Sailer[4], A. Erdmann[1,2,3]*
*[1] Erlangen Graduate School in Advanced Optical Technologies (SAOT), Germany;*
*[2] Friedrich-Alexander-Universität Erlangen-Nürnberg, LEB, Erlangen, Germany;*
*[3] Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany;*
*[4] Institut für Mikroelektronik Stuttgart (IMS CHIPS), Stuttgart, Germany*

**118** **14:00** **Photonic IC Lithography Software - Challenges and Solutions**

*N. Ünal[1], U. Hofmann[1], J. Bolten[2], T. Wahlbrink[2], A.-L. Giesecke[2], M. Hornung[2], J. Bolk[3]*
*[1] GenISys GmbH, Taufkirchen (Munich), Germany*
*[2] AMO GmbH, AMICA, Aachen, Germany*
*[3] Eindhoven University of Technology, NanoLab@TU/e De Zaale, Eindhoven, The Netherlands*

**120** **14:20** **Curvilinear Data Processing Methods and Verification**

*C. Browning, S. Postnikov, M. Milléquant, S. Bayle, P. Schiavone, Aselta Nanographics, Grenoble, France*

**122** **14:40** **A Resist Reflow 3D Compact Model Approach for Imager Microlens Applications**

*S. Bérard-Bergery[1], J. Hazart[1], P. Quéméré[1], C. Beylier[2], N. Allouti[1], M. Cordeau[1], R. Eleouet[1], F. Tomaso[1], J.-B. Henry[1], A. Ostrovsky[2], V. Rousset[2], V. Farys[2]*
*[1] ) CEA-LETI, Minatec Campus, Grenoble, France*
*[2] STMicroelectronics, Crolles, France*

**15:00-15:25 Coffee Break**

**Abstract Page**

**15:25-16:45**

**Session 9 – Mask2Wafer and Wafer2Wafer Metrology**

*Chair: J. H. Peters, bmbg consult, Radebeul, Germany*
*Co-Chair: F. Weisbuch, GLOBALFOUNDRIES, Dresden, Germany*

**124** **15:25** **Tilted beam SEM, a novel approach for industry 3D metrology**
*C. Valade[2], J. Hazart[1], S. Bérard Bergery[1], E. Sungauer[2], M. Besacier[3], C. Gourgon[3]*
*[1] University Grenoble Alpes, CEA-LETI, DTSI, Grenoble, France*
*[2] STMicroelectronics, Crolles, France*
*[3] University Grenoble Alpes, CNRS, CEA-LETI, LTM, Grenoble, France*

**126** **15:45** **On the Road to Automated Production Workflows in the Back End of Line**
*G. Tabbone, K. Egodage, K. Schulz, A. Garetto, Carl Zeiss SMT, Jena, Germany*

**128** **16:05** **Measuring inter-layer edge placement error with SEM contour**
*F. Weisbuch, J. Schatz, GLOBALFOUNDRIES, Dresden, Germany*

**130** **16:25** **FEM Simulation of Charging Effect during SEM Methodology**
*D. Duc Nguyen[1,2], J.-H. Tortai[2], M. Abaidi[1], P. Schiavone[1]*
*[1] ASELTA Nanographics, Grenoble, France*
*[2] CEA-LETI, Grenoble, France*

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**16:45-18:10**

**Session 10 – Using Big Data / Deep Learning**

*Chair: B. Le Gratiet, STMicroelectronics, Crolles, France*
*Co-Chair: S. A. Savari, Texas A&M University, College Station, TX, USA*

**134** **16:45** **Automatic Defect Classification of SEM images using Deep Learning (Invited)**
*L. Bidault, D. Mastroeni, STMicroelectronics Rousset, France*

**136** **17:10** **Deep Supervised Learning to Estimate True Rough Line Images from SEM Images**
*N. Chaudhary, S. A. Savari, S. S. Yeddulapalli, Texas A&M University, College Station, TX, USA*

**139** **17:30** **Microlens under Melt In-Line Monitoring based on application of Neural Network Automatic Defect Classification**
*J. Ducoté[1], A. Lakcher[1], L. Bidault[2], A.-R. Philipot[1], B. Le-Gratiet[1]*
*[1] STMicroelectronics, Crolles, France*
*[2] STMicroelectronics, Rousset, France*

**142** **17:50** **Machine Learning applications in overlay prediction**
*A. Lam, STMicroelectronics, Crolles, France*

**18:10** **Thanks to EMLC2018 participants & Announcement of EMLC2019**
*U. Behringer, UBC Microelectronics, Ammerbuch, Germany*

**18:15** **End of EMCL2018 Conference**

# Technical Exhibition

## during the

## 34th European Mask and Lithography Conference

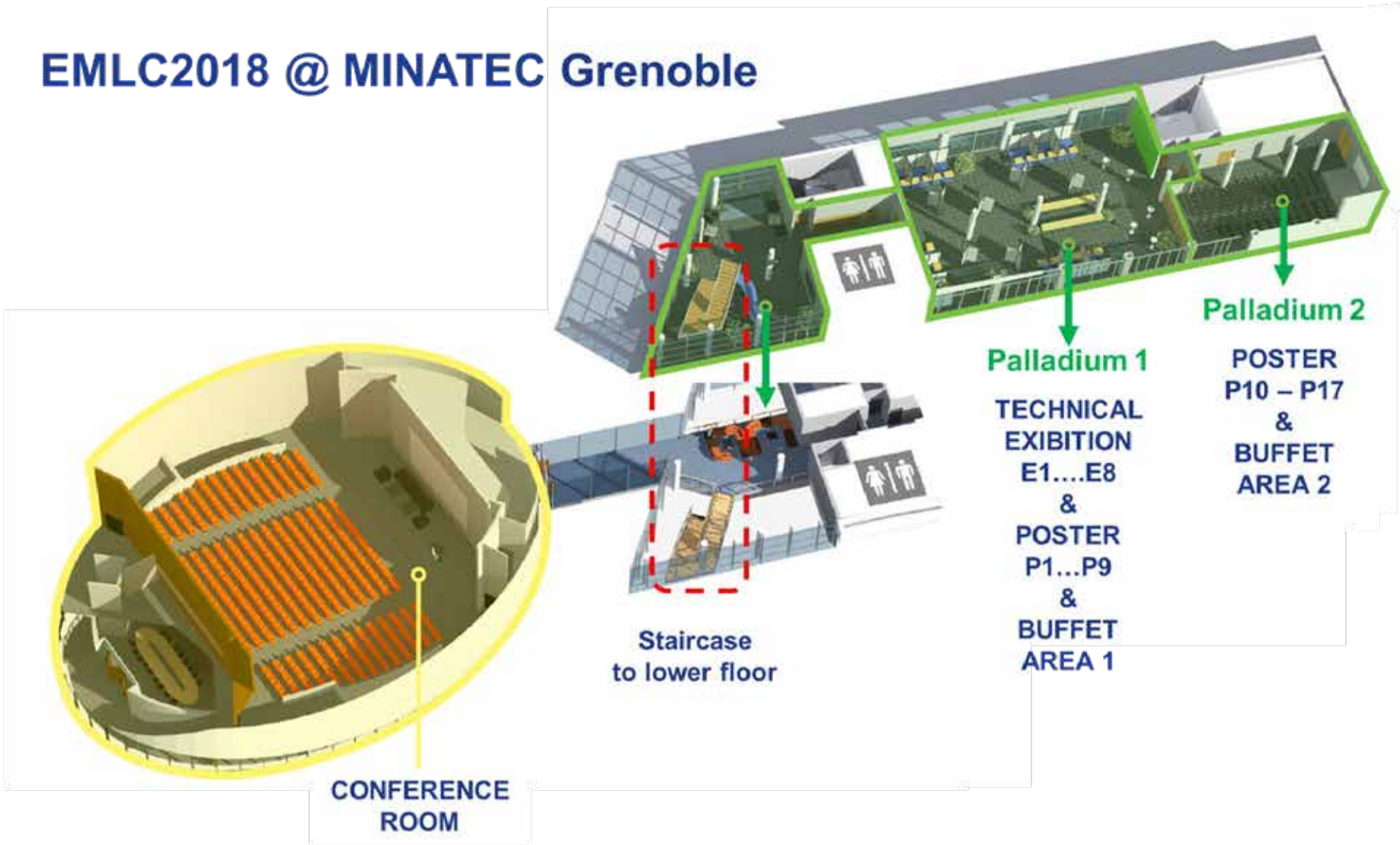
## EMLC2018

## June 18th – June 20th 2018

## MINATEC Conference Centre, Grenoble, France

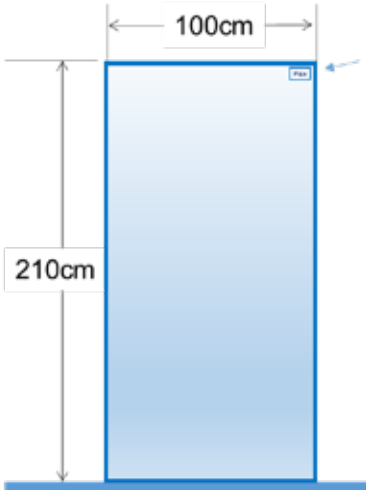
# *Exhibitor Information*

# EMLC2018 @ MINATEC Grenoble




# Floorplan Overview

## Poster Panel and Panel for Exhibition Booth (if ordered)




**Poster Number:**
**Px (x = 1, 2, ….., 17)**

**VELCRO tapes will be provided on site**
**for the Poster affixation to the Poster Panel**

**(!) No Pins (!)**
**are allowed to fix something onto a Poster Panel**
**or onto a Panel for an Exhibition Booth**


# Panel Layout

# Booth E1: Advantest

ADVANTEST

## Measure the Connected World

*And Everything in It*

## Technology Support on the Leading Edge

A world-class technology company, Advantest is the leading producer of automatic test equipment (ATE) for the semiconductor industry and a premier manufacturer of measuring instruments used in the design and production of electronic instruments and systems. Its leading-edge systems and products are integrated into the most advanced semiconductor production lines in the world. The company also focuses on R&D for emerging markets that benefit from advancements in nanotech and terahertz technologies, and has introduced multi-vision metrology scanning electron microscopes essential to photomask manufacturing, as well as a groundbreaking 3D imaging and analysis tool. Founded in Tokyo in 1954, Advantest established its first subsidiary in 1983 in Europe, and now has subsidiaries worldwide. More information is available at www.advantest.com.

www.advantest.com

# Booth E2: Systron

## Magnetically shielded rooms for Semiconductor Manufacturing

Systron EMV GmbH was founded 1993 and operates now offices in Germany and Switzerland. The core competences of Systron EMV GmbH include manufacturing, distribution and installation of passive and active systems to reduce low frequency magnetic fields. Furthermore, computer modeling of electrical systems and on-site measurements are carried in order to design and evaluate proper mitigation method. Systron's goal is to provide best possible solutions for the customer and to provide excellent service, prior, during and after finishing the project.

**Our goals**
Protecting highly sensitive equipment against electromagnetic and magnetic fields, for applications in research labs and semiconductor manufacturing.

**How do we achieve this?**

- Magnetically shielded rooms / Active compensation systems
- Magnetic field measurements / Modeling of electrical power systems

**Ebeam applications** such as lithography writers or electron microscopes are very sensitive to electromagnetic interference (EMI), and thus need to be protected from those unwanted noise. Today, two proven methods are widely accepted: passive shielding method with so called "Mu-Metal" plates and active cancellation systems with electronically controlled coils generating counter-fields to cancel unwanted noise. Often, both methods are combined to create cleanest possible environment.

**Unwanted magnetic noise fields** are emanated from remote sources such as railways, subways, overhead lines and tramways, but also from local generated fields, such as from transformers, switch gear or electrical cables. However, often underestimated, is the influence of moving metal objects such as from trucks, cars, elevators and even inside the room widely existing push carts.

**"Mu-Metal" shielded rooms** protect magnetically sensitive tools such as lithography writers, electron beam microscopes from unwanted magnetic noise fields and are even able to mitigate strong fields to uncritical levels.
"Mu-metal" is a clean metal and thus also perfectly suitable for clean room applications. The shielding properties of "Mu-Metal" neither wear out, nor is any kind of maintenance work necessary.

**Magnetic field measurement** allows qualifying rooms prior to tool move in. In case specs are exceeded, customized solutions, in order to reduce magnetic fields, can be provided. However, when tools are already productive, but show inexplicable behaviors, magnetic field measurement can help tracking down the source of the noise fields so actions can be taken to eliminate the source of the noise. Actions might include moving the source, shielding the source or the tool or adding compensation systems to cancel the noise.

**Germany**
Systron EMV GmbH
D-91126 Schwabach
www.systronemv.de

**Switzerland**
Systron EMV GmbH
CH-8635 Duernten

# Booth E3: CYBEROPTICS®

**® Auto Multi Sensor (AMSR) can measure humidity in all locations of the reticle environment. In immersion scanner environments for example, monitoring humidity is critical in reducing Reticle Haze. Haze is an adverse effect on reticles caused by a combination of Mask residue, 193nm light and H2O. AMSR can monitor humidity in the total reticle environment and detect any place where H2O is exposed to the reticle. AMSR speeds leveling, vibration and Relative Humidity (RH) When you need the world's most efficient and effective measurement devices for semiconductor tool set-up and maintenance processes, count on CyberOptics, the global market leader in wireless semiconductor measurement devices for chamber gapping, leveling, wafer handoff teaching, vibration, relative humidity and airborne particle measurement.**

**CyberOptics' ReticleSensemeasurement to help save significant time and expenses. Controlling particles, inclination, humidity and vibration are all important factors in ReticleSense measurement portfolio to enable improvements in fab yields and equipment uptime.increasing yield and reducing downtime.**

**Semiconductor fabs and OEMs value the accuracy, precision and versatility of the WaferSense and CyberOptics Corporation (NASDAQ: CYBE) is a leading global developer and manufacturer of high-precision sensing technology solutions. By leveraging its leading edge technologies, the company has strategically established itself as a global leader in high-precision 3D sensors. Headquartered in Minneapolis, Minnesota, CyberOptics conducts worldwide operations in through its facilities in North America, Asia and Europe.**

# Booth E4: Vistec

**Vistec Electron Beam GmbH**

**As a long-standing equipment supplier, Vistec Electron Beam GmbH is providing leading technology solutions for advanced electron-beam lithography. Based on the Variable Shaped Beam (VSB) principle, the electron-beam lithography systems are mainly utilized for semiconductor applications and advanced research as silicon direct write, compound semiconductor, mask making as well as integrated optics and several new emerging markets.**

**The company is located in Jena, Germany. In addition to its production facility in Germany, Vistec Electron Beam maintains service and support centers in Europe, USA and Taiwan.**

**Vistec Electron Beam GmbH**
**Ilmstr. 4**
**07743 Jena**
**Germany**
**Phone: +49 – 3641 – 7998 0**
**Fax: +49 – 3641 – 7998 222**
**Email: electron-beam@vistec-semi.com**
**Web: www.vistec-semi.com**

**Contact Person:**
**Mrs. Ines STOLBERG**
**Manager Product Management & Marketing**
**Phone: +49 – 3641 – 7998 155**
**Email: ines.stolberg@vistec-semi.com**

# Booth E5: Mentor Graphics


Mentor, a Siemens Business, is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world's most successful electronic, semiconductor and systems companies. We enable companies to develop better electronic products faster and more cost-effectively. Our innovative products help conquer complex design challenges.

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# Booth E6: GenISys

Based in Munich (Germany), with offices in Tokyo (Japan), and California (USA), **GenISys** develops, markets and supports flexible, high-performance software solutions for the optimization of micro- and nano-fabrication processes. Addressing the market for lithography and inspection, **GenISys** combines deep technical expertise in layout data processing, process modeling, correction and optimization with high caliber software engineering and a focus on ease of use.

**GenISys** products give researchers, manufacturers, and system suppliers unparalleled efficiency, ease of use and optimal value in research, development, and production of future nano-patterning technologies. As a company focused on customer service, **GenISys** delivers fast, highly dedicated support for the application and development of the functionality needed to meet demanding customer requirements.

## Products:

**Electron and Laser Beam Direct Write Software**

- Layout data preparation and PEC
- Market leader for Gaussian beam direct write systems
- Installed at most major nano-fabrication centers worldwide
- Has become a MUST for advanced e-beam lithography

**Monte Carlo simulation software**

- MC-Simulation for e-beam lithography simulation and correction
- PSF visualization, extraction and management
- Process Calibration

**3D lithography simulation software**

- Proximity Lithography (mask aligner, FPD exposure tools)
- Projection Lithography (stepper / scanner)
- Electron Beam Lithography
- Laser Beam Lithography (Heidelberg Instruments laser systems)

**SEM Image Analysis & Metrology**

- Metrology software for SEM images
- Automated feature size (CD) measurements
- Lines & spaces, circle, rectangle, gratings
- LER - line edge roughness analysis

# Booth E7: Pozzetta

**Pozzetta Inc**

**3121 S. Platte River Dr.**

**Englewood, CO 80122**

**USA**

**www.pozzetta.com**

**+1.303.783.3172**

**"We help our customers reduce costs with customized in-process solutions such as reticle boxes and reticle storage solutions, wafer carriers, and critical device shipping solutions. We help optimize fab space by personally reviewing the storage and processing of critical devices and delivering complete solutions that include RFID tags, reticle pods and custom cleanroom racks. We also help our customers by managing cleaning and maintenance programs for cassettes and pods."**

**Headquarters:** **3121 South Platte River Drive,**
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**Web Site:** **www.pozzetta.com & www.pozzettamicroclean.com**

**The products range of goes from the bare actuator or sensor to parallel-kinematic six-axis positioning systems and the integration of sub-components to complete system solutions.**

**Evaluation of test procedures, production processes and quality management are all included in the development process. The drive and positioning solutions from the PI Group often go beyond the state-of-the-art, providing customers with the competitive edge necessary to be successful on the market and always one step ahead.**

# Booth E8: XYALIS

**XYALIS**
**5 place Robert Schuman**
**38000 Grenoble**
**FRANCE**

www.xyalis.com
**Tel : +33 456 58 36 34**

XYALIS offers advanced solutions for Mask Data Preparation (MDP) and Design For Manufacturing (DFM) that shorten time to manufacturing, increase manufacturing yield, and remove errors during mask and wafer production. XYALIS solutions have been developed in cooperation with major semiconductor leaders and are being used in production for the most advanced technologies.

Established in 1998, XYALIS is headquartered in Grenoble with offices in San Jose-CA USA and Singapore. XYALIS is the leading specialist in layout finishing and GDSII/OASIS/OASIS.MASK processing software.
XYALIS focuses on two main flows of the layout finishing process: Mask Data Preparation and Metal Filling to address Chemical Mechanical Polishing (CMP) issues.

XYALIS offers a suite of tightly integrated state-of-the-art Mask Data Preparation modules that automate the repetitive and time consuming tasks between design and fracturing:

- Generation of Multi Project Wafers (MPWs) or shuttles with **GOTmuch**, an automated placement tool dedicated to maximizing silicon usage and minimizing saw lines when assembling heterogeneous chips,
- Generation of complex reticules with **GOTframe**, an automated tool for inserting manufacturing items between chips and inside scribe lines, according to reusable process rules,
- Intuitive mask set creation with **GOTmask**, supporting Multi-Layer Reticles (MLRs), optimized 1X flow, and wafer map optimization.

# Astracts

## 34th European Mask and Lithography Conference

## EMLC2018

## June 18th – June 20th 2018

## MINATEC Conference Centre, Grenoble, France

# Technology for Optical Sensors (Keynote)

Olivier Noblanc

STMicroelectronics, Crolles, France

CMOS technologies are now widely used in the frame of Image sensors serving a large field of application (consumer, industrial, automotive…) leveraging on the easy access to silicon facilities and availability of software IPs suitable to realize both the CMOS Image Sensors (CIS) and Image Signal Processor (ISP) devices.

The trend to pixel size scaling which have been driving the industry since a while in order to increase the resolution of images in mobile devices is now slowing done with pixel size in reaching the 1µm² or so.

New kinds of pixel and related technologies enabling plenty of other kind of applications are now investigated by many companies. In this field the diversity of pixel sizes and architectures is increasing creating some new challenges for silicon technologist. Lithography and all other process activities are proposing innovative features aiming to offer the best technologies for the targeted products.

STMicroelectronics is deeply involved in this race to innovation proposing a wide range of technologies. The goal of this talk is to summarize some recent developments and the new process features that have been put in place in Crolles facility in order to serve these emerging markets.

# Transparent and conductive backside coating of EUV lithography masks for Ultra short pulse laser correction

**Rinu Abraham Maniyara[1], Dhriti Sundar Ghosh[1], Valerio Pruneri[1,2]**

1. **ICFO - Institut de Ciències Fotòniques, The Barcelona Institute of Science and Technology, 08860, Castelldefels, Barcelona, Spain**
2. **ICREA - Institució Catalana de Recerca I Estudis Avançats, 08010 Barcelona, Spain**

Photolithographic masks especially for extreme ultraviolet lithography (EUVL) have to fulfill demanding requirements with respect to critical dimension (CD) uniformity, mask flatness, and especially image placement (registration) as well as mask-to-mask overlay. These challenges require highly precise techniques for the production of extreme ultraviolet (EUV) masks. It is already known that an optical photomask can be modified in a controlled manner in order to correct image placement signatures by applying ultra-short laser pulses into the substrate by using the RegC system. This compensation occurs through multiphoton absorption of incident light from the backside of the mask. Applying this technology to EUV masks thus requires a backside coating sufficiently transparent at the wavelength of the ultra-short laser pulses.

On the other hand, an extremely careful handling and chucking of EUV mask is necessary in order to avoid as much as possible mechanical abrasion and the formation of particles, which may deteriorate the function of an EUV lithography system. In order to fulfill these handling requirements, EUV mask are held through an electrostatic chuck in the scanner. As the substrate of EUV masks is a dielectric, usually glass, or a semiconducting material, an electrically conducting layer has to be deposited on the backside in order to be able to hold the substrate with an electrostatic chuck. Therefore, in order to allow image placement correction by ultra-short pulse laser technology, the rear side coating has to be optically transparent and electrically conductive at the same time.

Ultrathin metals, their nitrides and oxides, borides, carbides or combinations, if sufficiently thin become transparent while still being electrically conductive. We will present results on backside coatings for lithography masks, especially for EUV applications, consisting of multilayer films made of ultrathin Cr, Cr nitrides and oxides having different compositions and thicknesses. Different compositions are obtained by varying the atmosphere during deposition. For example, during deposition of the Cr atoms on a substrate one can obtain different $CrN_y$ compositions by a

proper ratio of $N_2$ and Ar during the sputtering process. Though we show results on Ni and Cr, the concept can be extended to any other suitable metals and combinations of nitrides, oxides, borides, and carbides of proper stoichiometry.

In the talk we will present our studies that confirm the possibility to achieve an optically transparent (transmission of 20-50%) and electrically conductive (sheet resistance of 50-200 ohm/sq.) backside coating for lithography masks with high mechanical resistance and durability, the latter attributes being tested also through abrasion, adhesion and scratching tests. We will also demonstrate pixel writing through such coating, enabling the technological path to correction and tuning of image placement on EUV masks.

# THE BATTLE FIELD OF LITHOGRAPHY

Laurent Pain[a]

[a]*CEA-Leti Minatec Campus 17, Rue des Martyrs F-38054 Grenoble, France*
Email : laurent.pain@cea.fr

Lithography is and will remain the key knob for the development and ramp-up of semiconductor technology. Depending the challenge of the device design rules, the patterning strategy drives the future architecture definition and associated performances of our devices. On this landscape, optical lithography represents the reference lithography solution. Resolution and nowadays alignment performances remains the strategic keys from the process side. However, when cost of ownership starts to be taken into account, final decision of the manager has to be pragmatic. In that context, optical lithography has some technology challengers as alternative patterning techniques may have a high-level of competitive advantages. They could indeed offer challenging and credible industrial compromises. Among them,

- The launch of massively parallel mask less lithography is without any doubt an attractive solution for the semiconductor industry and opens new opportunities for the manufacturing of innovative chips. Now MAPPER production platform is on the path to industrial ramp-up with operational active blanker.
- UV flash imprint (NIL) in step and repeat mode or at full wafer scale level is also another one of these promising alternatives that offers a large versatility. It can address a large growing demand.
    - The most advanced semiconductor technology nodes supported by CANON
    - A large field of applications such as photonic, bio and optical sensors, lighting, display, photovoltaic. For those technologies, the full wafer-scale imprint strategy may represent a good compromise.
- Directed Self Assembly by block copolymer is THE complementary patterning solution by excellence that can push very far any type of lithography solution : EUV, 193, ML2, NIL. PS-PMMA platform is already a mature platform and the new high-chi generation is under active development.
-

Taking concrete example issued from the Leti R&D environment, this talk will engage the discussion to position each alternative with respect to the optical lithography reference. The objective will be to present a good and fair overview to understand when and how these technologies could be attractive and become real industry references. Even if they are competitive on the paper, they can also present a lot of synergy for the development of affordable technological options for tomorrow.

# Multi-Beam Mask Writer – Enabling Tool for EUV Lithography

Patrick Mayrhofer, Christof Klein, and Elmar Platzgummer

IMS Nanofabrication GmbH
Schreygasse 3, 1020 Vienna, Austria

This presentation will give an overview of recorded tool performance data and availability. In addition, specific benefits of multi-beam writing by using curvilinear “ideal” ILT (inverse lithography technology) for EUV masks will be discussed.

IMS Nanofabrication’s MBMW-101 (Fig. 1) multi-beam mask writer is already recognized as a value-adding tool in the mask shops of several important members of the high end mask industry.

The reliability in operation has been demonstrated, in particular the multi-beam generator (aperture plate system) and the data path have shown a high degree of stability: Virtually no lifetime limiting factor for the key components has been found.

Multi-beam writing has proven to meet industry expectations in terms of enabling a higher exposure dose for low sensitivity resists to ensure low LER (line edge roughness) and high pattern fidelity. MBMW series mask writer can handle enhanced pattern complexity without productivity tradeoff and accelerating cycle time. In fact, multi-beam mask writers are required to keep mask write times for leading-edge advanced layouts well below 24h.

Both CDU (critical dimension uniformity) and Registration (pattern placement accuracy) do not only meet the targeted 7 nm mask node requirements, as with recent tool improvements also 5 nm lithography requirements can be met. For instance, the introduction of a novel thermal expansion correction is leading the way to unprecedented placement accuracy across the complete mask area.

Hence, MBMW-101 has already become the preferred, if not the only practical solution for 193i ILT [1], NIL master template [1,2], and EUV mask writing.

The superior properties of multi-beam mask writer tools in terms of high resolution and simultaneously high throughput, even when realizing curvilinear patterns (Fig. 2), are enabling cost effective EUV mask writing.

References:

[1] Hiroyuki Miyashita et al., “Practical performance evaluation of MBMW-101 for mask production”, Dai Nippon Printing Co., Ltd., presented at SPIE Advanced Lithography 2018, San Jose, California, USA

[2] Koji Ichimura et al., “Fabrication of full-field 1z template using multi-beam mask writer”, Dai Nippon Printing Co., Ltd., presented at SPIE Advanced Lithography 2018, San Jose, California, USA


| | |
|---|---|
| Beams | 262,144 programmable beams |
| Beam energy | 50 kV |
| Platform | JEOL platform with air-bearing stage |
| Mask write time for 7nm node | <10h (104mm x 132mm) |

Fig. 1: IMS MBMW-101

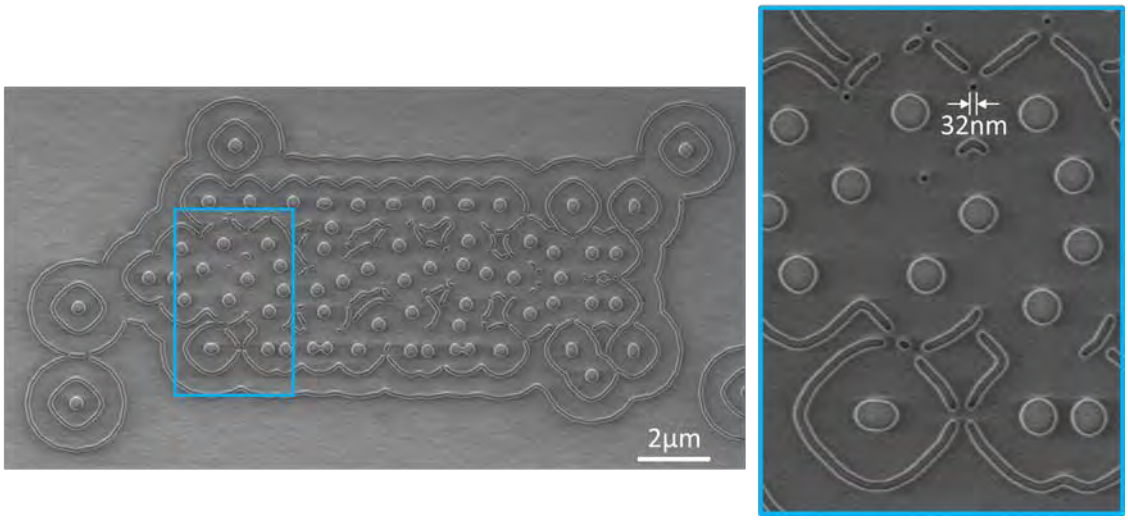


Fig. 2: Curvilinear ILT (Inverse Lithography Technology) test pattern

# Multi-beam mask writer MBM-1000 for advanced mask making

Hiroshi Matsumoto, H Yamashita, Hironobu Matsumoto, N. Nakayamada.

NuFlare Technology, Inc. (Japan)
8-1 Shinsugita-cho, Isogo-ku, Yokohama, Kanagawa 235-8522, Japan
Phone: +81-45-370-9244 FAX: +81-45-370-9974 e-mail: matsumoto.hiroshi@nuflare.co.jp

Shrinkage of semiconductor devices has slowed down, but strong motivation for further shrinkage persists. ArF immersion lithography has been extended by introducing multiple patterning technique and aggressive OPC, and finally production by EUV lithography is about to start. Advanced lithography is posing challenges of writing accuracy and large figure count for mask writer.

For leading-edge mask making, single variable shaped beam (S-VSB) writer has been used as it has high TPT and good resolution with VSB system. We have released EBM-9500[1] for N7 lithography, with high current density of 1200 A/cm$^2$, thermal effect correction and fast three-stage deflection system. However, perpetual extension of VSB writer throughput seems technically difficult, and multi-beam writers are claimed to be essential for EUV lithography.

We have developed a multi-beam mask writer MBM-1000 for N5 production. It is based on large area projection optics with blanking aperture array (BAA) for individual beam blanking as shown in Fig. 1. For patterning resolution, it uses 10-nm beam size and new optics with smaller aberration. Writing results demonstrates better resolution of MBM-1000 than EBM-9000 [1].

To further extend patterning resolution, pixel level dose modulation (PLDC) is developed for MBM-1000. It modulates exposure dose pixel by pixel, to enhance dose contrast at pattern edge[2]. It improves CD linearity, pattern fidelity and enlarges dose margin. PLDC runs inline in parallel to writing, and thus does not require calculation before writing.

PLDC also corrects linearity, and effectiveness of correction is evaluated by simulation as shown in Fig.2. CD linearity is corrected even without extra dose modulation, and dose margin is improved with additional dose modulation of 140%, and further improvement is gained with 200% dose modulation. User can specify maximum dose modulation allowed for PLDC to balance correction gain and write time increase. According to the simulation result, 140% modulation is a good condition balancing write time increase and linearity correction gain by dose modulation.

## REFFERNCES

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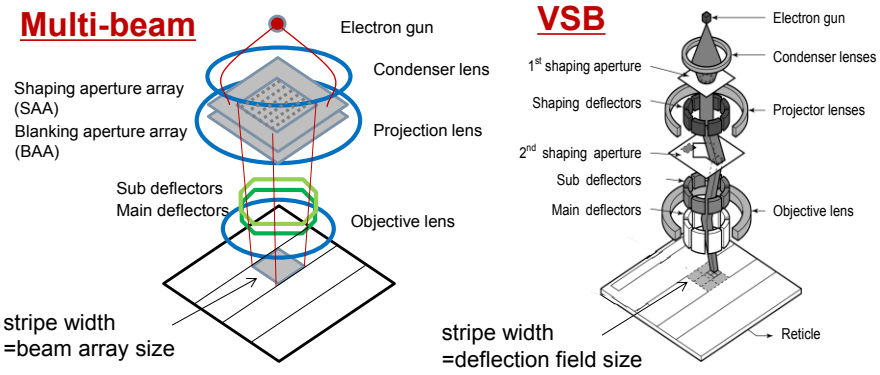
[2] Zable H., Matsumoto H., Yasui K., Ueba R., Nakayamada N., Shirali N., Masuda Y., Pearman R., Fujimura A., "GPU-accelerated inline linearity correction: pixel-level dose correction (PLDC) for the MBM-1000," Proc. SPIE 10454, 104540D-1 (2017).




| | MBM-1000 | EBM-9500 |
|---|---|---|
| beam size | 10 nm beam in 512×512 array | variable 350 nm |
| current density (A/cm$^2$) | 2 | 1200 |
| max. total current (nA) | 500 | 700 |
| stripe width (um) | 82 (beam array size) | 81 (deflection field size) |

Figure 1: Configurations of MBM-1000 and EBM-9500

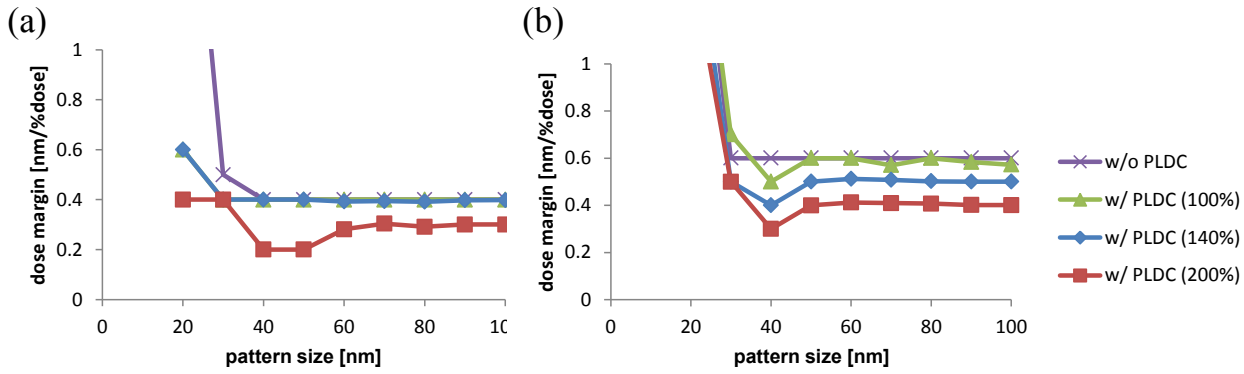



Figure 2. Dose margin (dose latitude) of line and space pattern with (a) 5% density and (b) 50% density simulated with threshold dose model.

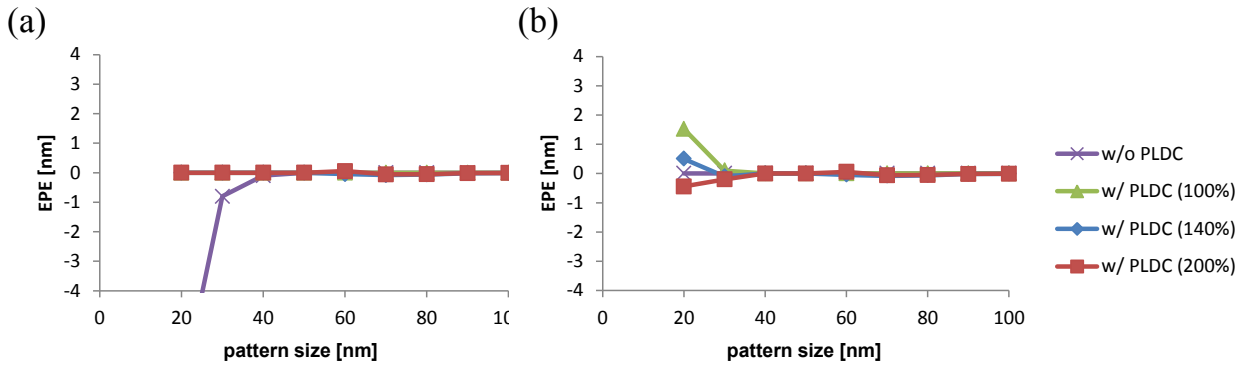



Figure 3. Edge placement error of line and space pattern with (a) 5% density and (b) 50% density simulated with threshold dose model.

# Multi-Trigger Resist for Electron Beam and Extreme Ultraviolet Lithography

C. Popescu[a,b], A. McClelland[c], G. Dawson[c], J. Roth[d], A.P.G. Robinson[b,c]

[a]*Nanoscale Physics, Chemistry and Engineering Research Laboratory, University of Birmingham, UK.*
[b]*School of Chemical Engineering, University of Birmingham, UK.*
[c] *Irresistible Materials Ltd, Birmingham, UK*
[d]*Nano-C, Westwood, MA, USA.*

Remarkable progress has been made in the semiconductor industry with advances in integrated circuit technology. This has been driven by development of lithography techniques capable of high resolution patterning, which include EUV, DUV, and electron beam, and also new generations of high-resolution high sensitivity resist materials.

Extreme ultraviolet lithography (EUVL) at 13.5 nm is the most likely to be the chosen post-optical technique for patterning sub 20 nm half-pitches for chip manufacturing, [1] with high-volume manufacturing deployment expected imminently. Along with addressing issues regarding the availability of EUV power sources, the most challenging necessity in promoting the EUVL as industrial lithographic technique for high-volume production has been the need for improvement of resist performance, or the development of novel resist materials capable of meeting industry requirements for ultimate resolution while maintaining a good sensitivity and low line edge roughness. [1]

Whilst efforts are to develop candidate EUV resists there is another non-trivial factor to consider in this process: mask production. The increase in the resolution of the main exposure tools currently being used for high-volume production of semiconductor devices has pushed the resolution of the chemically amplified resist used in electron beam mask writers towards 16 nm half-pitch. [2] Direct-write electron beam mask patterning is an indispensable technology owing to its fine focusing characteristics and high precision spatial control of charged particles, which photolithography does not posses. However, direct-write is time-consuming unlike projection exposure in the photolithography. It requires highly sensitive resists in order to reduce the patterning time of complicated mask patterns. In addition to sensitivity, the roughness of the developed resist sidewall also plays an important role in the fabrication of photomasks and molds. [2]

Traditional resists have enabled a half-pitch of 22 nm in production. However, chemically amplified resists can naturally limit the ultimate resolution in the resist due to acid diffusion, and to post exposure instability in the patterned regions. [1] In addition, for sub 10 nm patterning the LER and LWR become critical parameters that put an additional constraints on chemically amplified resist. Recently, attention has focused on the development of non-chemically amplified resists for lower lithography nodes, such as an MAPDST-MMA copolymer that contains a sulfonium group to give their material the sensitivity for electron beam radiation. A resolution of 20 nm in 1:2 line/space patterns was achieved. [1]

We are working on the development of a new negative tone molecular resist platform for electron beam lithography as well as extreme ultraviolet and optical lithography. We have previously reported the performance of the xMT resist, which shows a good combination of sensitivity, low line edge roughness and high-resolution patterning. [3] In order to overcome the limitations induced by acid diffusion we have recently investigated and introduced a new mechanism in our resist, named the multi-trigger concept.

In a Multi-Trigger Resist, multiple distinct chemical reactions must take place simultaneously and in close proximity for the amplification process to proceed. Thus, at the edge of the feature, where the density of photo-initiators that drive the chemical reactions is low, the amplification process is self-terminating, rather than requiring a quencher. This significantly reduces blurring effects and enables much improved resolution and line edge roughness while maintaining the sensitivity advantages of chemical amplification. Here we present results obtained so far where the behaviour of the resist is driven towards the multi-trigger regime by manipulating the resist formulation. We demonstrate a resolution of 13 nm half-pitch in semi-dense (1:1.5 line/space) and 22nm diameter pillar patterns in electron beam and 16 nm half-pitch resolution in dense (1:1 line/space) patterns in EUV using the MTR material with an improvement in the LER value in the higher MTR formulations.

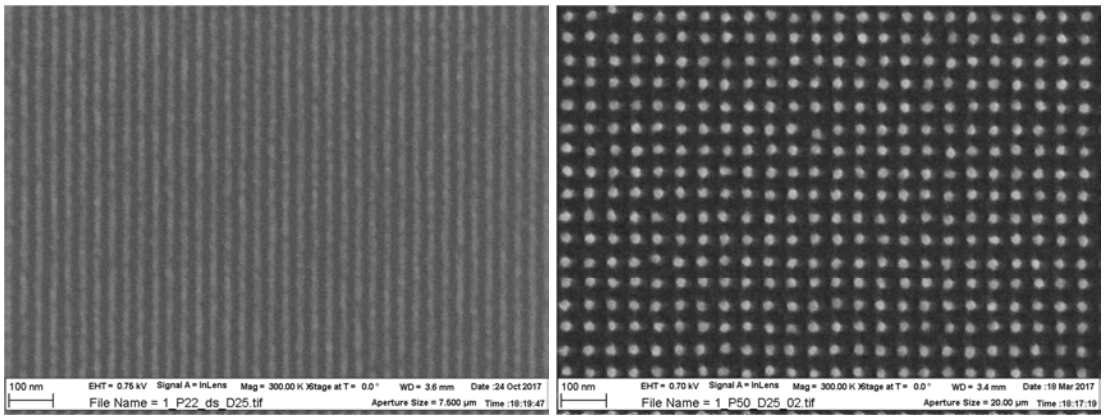



**Fig.1** SEM images of patterned MTR resist in electron beam lithography a) CD 13.0nm at pitch 33nm, LER 5.8nm, b) pillars diameter 22.6nm at pitch 50nm

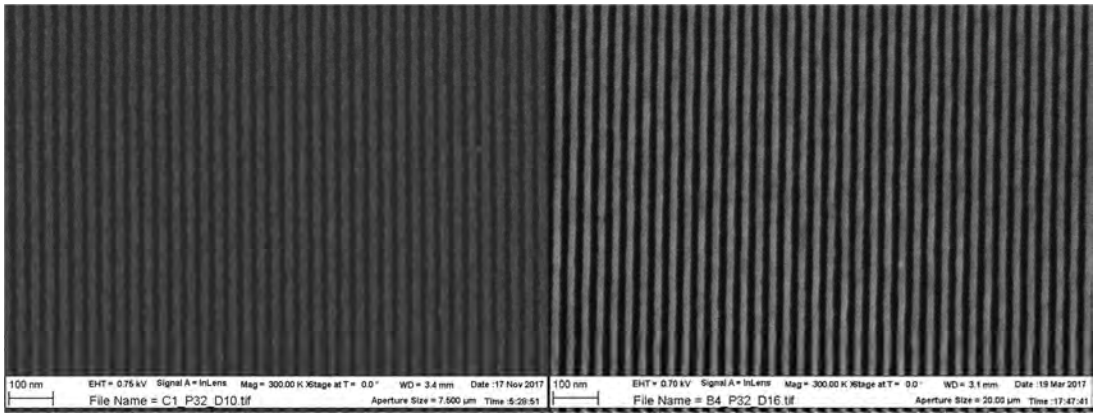



**Fig.2** SEM images of patterned resist in EUV lithography: a) standard MTR formulation, 46mJ/cm$^2$, CD 15.8nm, LER 3.86nm b) higher MTR formulation 47.4mJ/cm$^2$ CD 14.6nm, LER 2.06nm

## References

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# Photonic superlattice multilayers for EUV lithography infrastructure

F. Kuchar and R. Meisels*
*Institute of Physics, Montanuniversität Leoben, 8700 Leoben, Austria*
*meisels@unileoben.ac.at

The extreme ultraviolet (EUV) is considered as crucial for next-generation lithography, i.e. transistor gate lengths of 7 nm or less [1]. Most EUV lithography systems use a plasma source whose emission peaks at a wavelength $\lambda$ of 13.5 nm. This wavelength is 14 times shorter than the wavelength of 193 nm used in present-day lithography systems promising greatly improved resolution.

A typical EUV lithography (EUVL) system consists of the EUV source, a collector, illumination optics, a pellicle, a reflective EUV mask, projection optics and finally a resist-coated wafer. A presently widely used EUV source – a $CO_2$ laser excited tin plasma – has a bandwidth (FWHM) of about 1 nm. The goal for the bandwidth of the illuminating radiation is 2% at 13.5 nm, i.e. approx. 0.3 nm.

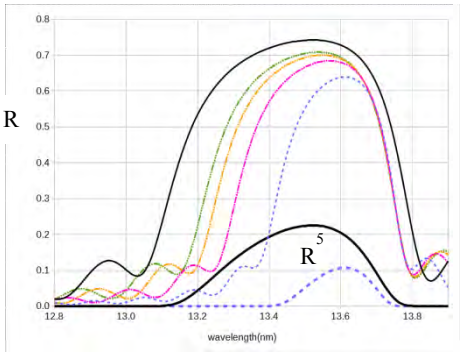
In the optical path several mirrors are used, altogether approximately ten. The reason for using mirrors is that at 13.5 nm the refractive index of all chemical elements is governed by atomic-core level transitions and the value of its real part $n$ is close to unity. Therefore, simple refractive elements like lenses cannot be designed. Mirrors, however, can be made on the basis of Bragg's law by employing the constructive interference of multi-layers with the index ($n$) contrast of two consecutive layers as large as possible but with little absorption (imaginary part of the refractive index). These Bragg reflectors are the established choice for most of the reflecting elements in the system.

The "standard" Bragg reflector with reflectance $R$ of about 0.74 at normal incidence uses 40 to 50 double layers of molybdenum and silicon. At 13.5 nm Mo has a relatively strong deviation ($\delta$= -0.076) of $n$ from 1. Si behaves almost like vacuum ($\delta$= -0.001), yielding the necessary index contrast. The values of the imaginary parts $\beta$ of $n$ are 0.0064 and 0.0018 for Mo and Si, respectively. This causes weak but not negligible absorption and restricts the number of useful Mo/Si double layers to 40 – 50. The period of this standard Mo/Si Bragg mirror is 6.9 nm. For optimal reflectance the thickness of the Si layer is 60% of the period.

Various concepts of modifying the "standard" Bragg mirror have been reported in the literature, reviewed in [2]. In the present work we investigate the basic properties and possible applications of modified "standard" Bragg reflectors by numerical modelling. In the first step we superimpose a superlattice. It means the superposition of a superstructure on the basic one-dimensional periodic structure by replacing one element in certain layers periodically by another element, e.g. in every fifth double layer of the Mo/Si multilayer Mo is replaced by Si ("SL-5"). This is a well-known concept in semiconductor physics. In the second step we combine two different superlattice structures, e.g. SL-4 and SL-5. The third step is a variation of the period with depth. In these depth-graded multilayers light of different wavelengths is reflected at different depths in the stack. In the fourth step we take variable widths of the EUV source spectrum into account. We weight the reflectance with the spectrum within this width.

The reflectance of the multilayers is calculated by means of the multiple scattering method (MSM) using the MULTEM2 program [3]. It calculates the scattering transfer matrix for each individual element and determines the total scattering matrix as the product of the individual matrices. This matrix is used to output transmittance, reflectance, and absorbance. The MULTEM2 program was modified to take into account the wavelength dependence of the complex dielectric permittivity $\varepsilon$ (related to the complex refractive index) [4]. For Mo and Si the permittivity was calculated from the atomic structure factors $f_1$ and $f_2$ available from [5].

The main results of our numerical study obtained on the superlattice multilayers, which cannot be produced with the "standard" Mo/Si Bragg mirror, are: 1) Narrowing of the bandwidth of the normal-incidence peak with only slight reduction of the peak reflection (Fig.1). Maintaining a high reflectance is an advantage over other concepts for reducing the bandwidth. Multiple reflections on the mirrors in the optical EUVL system reduce the peak reflectance and narrow the peak width. Examples for five reflections ($R^5$) are shown for the "standard" and the superlattice-2 mirror. The FWHM is 0.61 and 0.35 nm, resp., after one reflection and 0.42 and 0.21 nm, resp., after five reflections. 2) Filling the reflection gap (Fig.2(a)) between near-normal incidence and total reflection with reflection peaks at certain angles, Fig.2(b). Their number is increased with increasing superlattice number and when combining different superlattices. 3) Depth grading of the periods of the combined superlattices even leads to reflection at all the angles where it is zero in the "standard" mirror, Fig.2(c). However, it is accompanied by a reduced but broader reflectance of the near-normal incidence peak and minima with about one percent reflectance at a few angles. 4) Weighting the reflectance with the spectrum of a EUV source [6], $\langle R \rangle$, smoothens the angle dependence and leads to all-angle reflection, Fig.2(e). In this figure two different widths are considered. Other spectra and different widths can easily be taken into account. Below the onset of total reflection $\langle R \rangle$ values are between 0.07 and 0.28 depending on spectral width and angle, Fig.2(e).




| |
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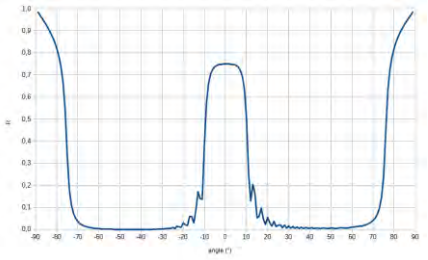
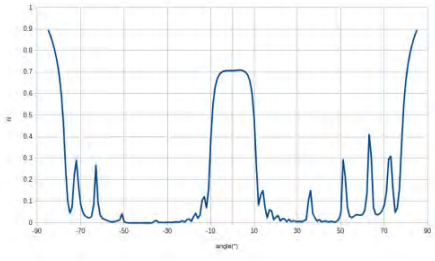
Fig.1. Left: Reflectance *R* at normal incidence of Bragg mirrors with SL-2 (blue), SL-3 (red), SL-4 (yellow), SL-5 (green) and without superlattice (black). The number of double layers is 80, 60, 53, 50 and 40, respectively. This way the number of Mo/Si interfaces is constant (40). Lower black and blue curves are for five reflections. Right: Example for the layer structure (superlattice-3).


(a)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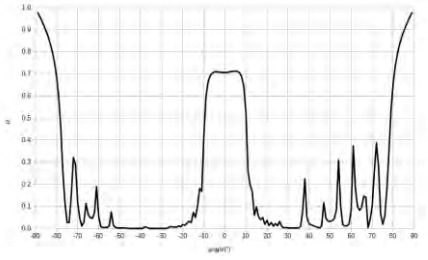
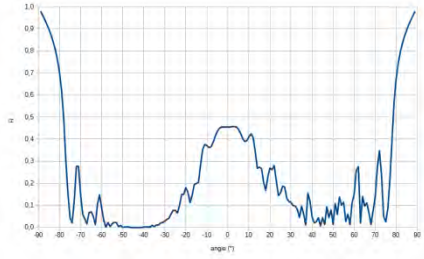

(c)


(d)

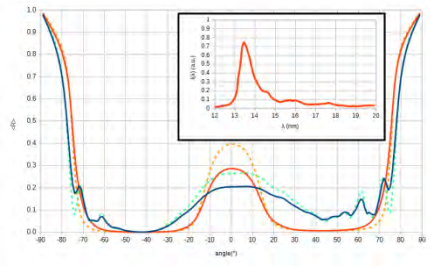

(e)

Fig.2 Reflectance as a function of angle of incidence at 13.5 nm: (a) "standard" Bragg mirror, (b) SL-5, (c) SL-5+SL-4, (d) SL5+SL4 with depth grading, (e) Reflectance <*R*> weighted by the Sn emission spectrum of Ref.6 (insert). Full curves: spectral width 12 – 20 nm (blue: graded SL-5+SL-4; red: "standard" mirror). Dashed curves: spectral width 13 - 15 nm (green: graded SL-5+SL-4, red: "standard"). Positive (negative) angle: s (p) polarization.

From result 1) EUV optical systems can benefit where a narrow-band mirror response is needed. This could be in EUV lithography or in monochromators. Results 2) and 3) allow multi-angle, equivalently multi- or broadband-wavelength applications where maximum reflectance is not required, e.g.in EUV spectroscopy or metrology for EUV sources, and higher integral reflectivity in the combination with a broad-band EUV plasma source. Result 4) shows that different parts of the EUV source spectrum can be used at different angles of incidence enhancing the weak all-angle reflection of the graded combined superlattices without weighting.

Regarding the structural design, Bragg mirrors with superlattices are simple modifications of the constant-period "standard" Bragg mirrors. Compared to the latter ones, in the simplest case, only certain layers of one element have to be replaced by layers of the other element without changing the basic double-layer thicknesses and period. With depth grading the modification also means a variation of the period.

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# EUV Pellicle Update

Jan-Willem van der Horst, Derk Brouns, Par Broman,
Raymond Lafarre, Theo Modderman, and Guido Salmaso

ASML Netherlands B.V., Veldhoven, The Netherlands

**Keywords:** EUV, pellicle, reticle defect mitigation, EUV mask infrastructure

Over the past years, ASML has taken the EUV pellicle from the concept level to pilot production and subsequently to a product that is being shipped to EUV customers, and being used in EUV scanners. Tooling is available to mount and demount pellicles to EUV masks.

To enable defect free imaging today's pellicles have zero defects larger than 25um, and single digit defects in the 10-25um range, as is shown in Figure 1. Several pellicles with zero defects > 10um have been manufactured

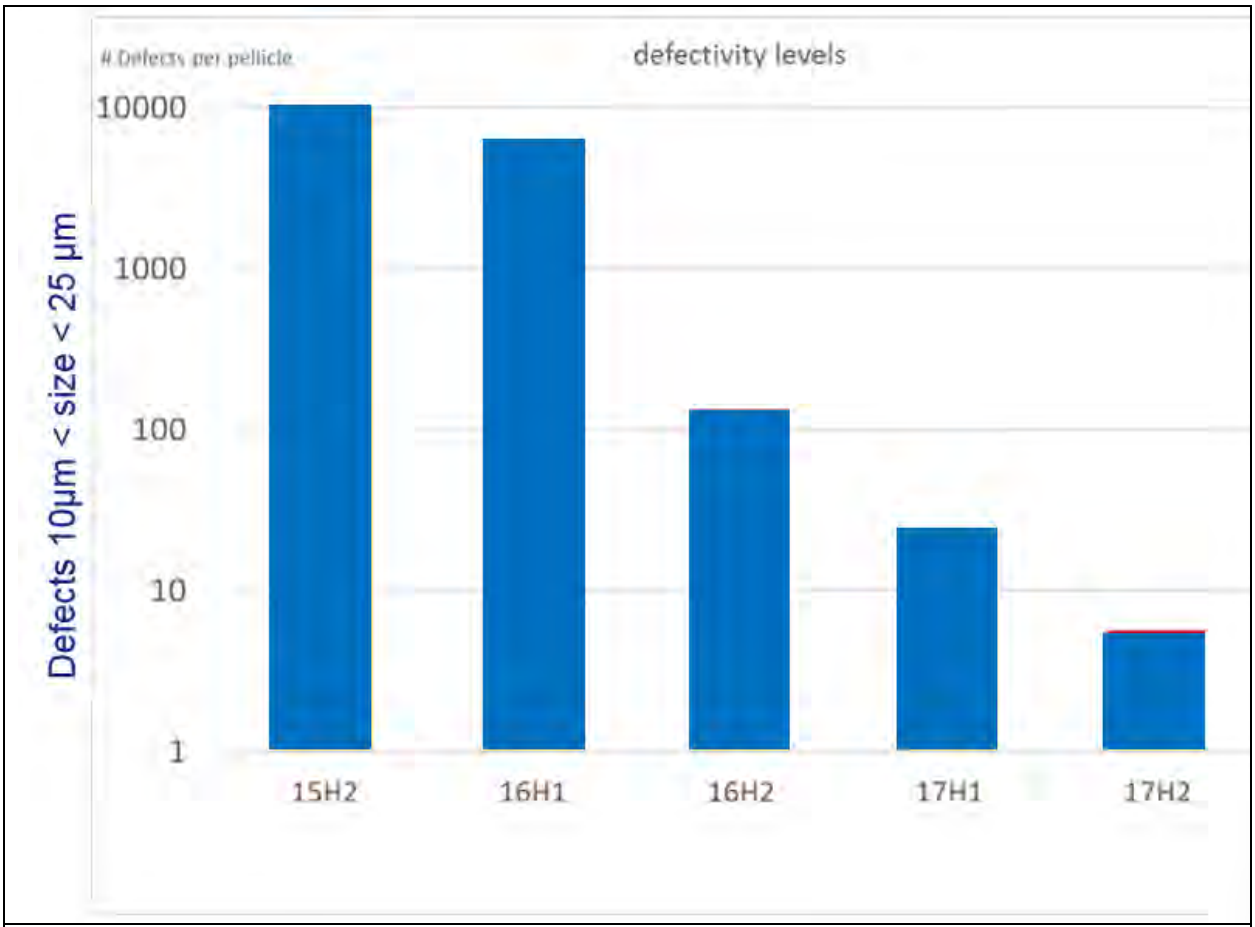



Figure 1: pellicle defects levels reducing from several thousands early 2016 to <10 by late 2017.

Full size pellicles with single pass transmission in the 78-80% range are regularly available and testing of >83% transmission pellicles has started. Pellicle stack selection for the next generation > 88% has started.

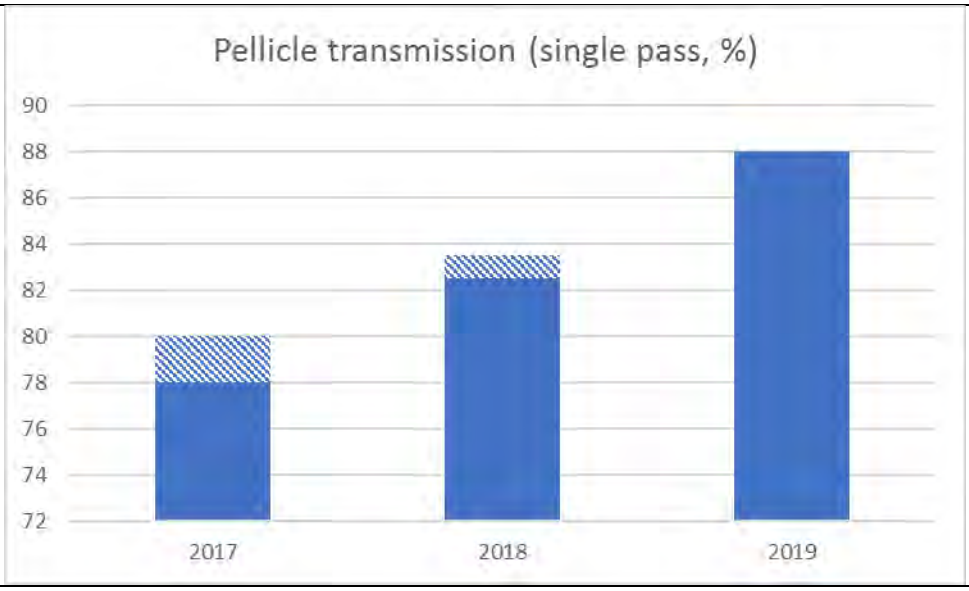



Figure 2: Pellicle transmission evolution from 78-80% range to ~83% and planned transmission for 2019 of 88%.

Apart from pellicle-level performance, we will also show in-scanner performance, such as CD uniformity impact of the pellicle, and pellicle endurance test results.

# NXE:3400B imaging performance assessed from a customer perspective

Guido Schiffelers, Friso Wittebrood, Colette Legein

ASML Netherlands B.V., Veldhoven, Netherlands

With the introduction of the NXE:3400B EUV scanner, ASML brings EUV lithography to the standards required for High Volume Manufacturing (HVM). Where the previous tools were accepted and assessed by research and pre-development organizations at our customers, the NXE:3400B scanner is accepted as HVM scanner by process development organizations at our customers.

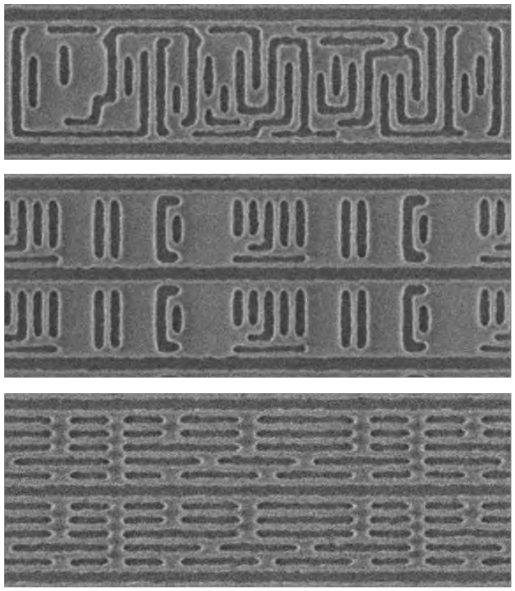
This transformation comes with the obligation for ASML to thoroughly assess, qualify and verify the NXE:3400B scanner performance according to our customers' HVM requirements. The value of bringing in the customer perspective into the performance assessments is to understand the imaging challenges our customers will face in an early phase, enabling better support during HVM ramp up.

This presentation will demonstrate the performance of the NXE:3400B as an HVM scanner, with a focus on imaging performance for customer use cases, based on the on-wafer imaging performance metrics CDU, local CDU (contrast), proximity matching and pattern shift. EUV industrialization will first take place for Foundry Logic Metal layers, followed by IDM Logic and DRAM. An imaging assessment will be presented for Foundry logic Metal layers, 'IDM' dark-field block mask application and 'DRAM' regular and staggered contact holes

## Logic Metal layers

a. Single expose

The 'foundry logic' imaging cases include dense and isolated lines & spaces, semi-isolated two-bar, tip to tip & tip to line and small metal clips (1D & 2D).
For two bar trenches, the top vs. bottom dCD variability can be reduced significantly by phase-corrected SMO, which takes into account the two-bar's intrinsic sensitivity to odd aberrations.
Tip to tip data shows the potential of pupil and OPC to print tip to tip down to the customer requirements.
The logic use cases are assessed for a variety of illumination settings covering projected customer use, which enables on wafer assessment of illumination dependencies on Aberration effects.
We will also discuss how we can deal with the challenges to improve the stochastical resolution limit for single exposure, which is currently limited around $k_1 \sim 0.4$.



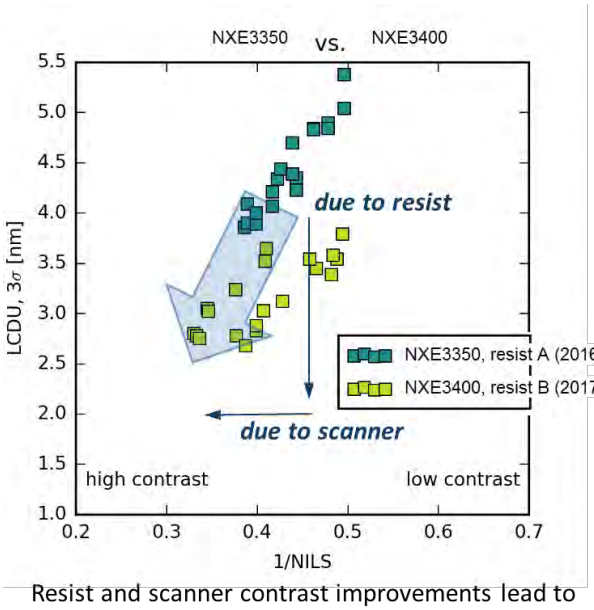
Printability assessment for logic metal clips

b. Non-Single expose ('block mask')

As an alternative patterning solution for metal, an EUV block mask patterning solution will be showcased. In this process, the final metal pattern is generated by a double patterning approach, where first a grating is patterned which is subsequently 'cut (or blocked)' by a second patterning step using a block mask with EUV, to create the final critical tip-to-tip dimensions in the grating.

**‘DRAM’ regular and staggered contact holes**

By on-wafer verification of local CDU improvements on contact holes, we will demonstrate the benefit of the extended illuminator flexibility of the NXE:3400B in terms of contrast and thus local CDU, as well as the need for further developments on resist platforms to improve both dose and local CDU performance.




Resist and scanner contrast improvements lead to reduced Local CDU

# Reticle CDU improvement by Zeiss CDC and the impact on real circuit pattern

Rolf Seltmann*[a], Thomas Thamm[a], Bernd Geh[d], Marija Djordjevic Kaufmann[b], Alla Bitensky[c], Aravind Narayana Samy[a], Stephanie Maelzer[a], Martin Sczyrba[e]

[a]GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, Wilschdorfer Landstr. 101, 01109 Dresden, Germany
[b]Carl Zeiss SMT GmbH, Rudolf-Eber-Str. 2, 73447 Oberkochen, Germany
[c]Carl Zeiss SMS, HaDolev 3, P.O. Box 32 Bar Lev Industrial Park, D.N. Misgav 2015600, Israel
[d]Carl Zeiss SMT, c/o ASML Technology Development Center, 2650 W. Geronimo Place, Chandler, AZ 85224, USA
[e]Advanced Mask Technology Center GmbH & Co. KG, Rähnitzer Allee 9, 01109 Dresden, Germany

## ABSTRACT

The excellent control of the critical dimension (CD) is an essential pre-requisite for a defect free patterning at advanced technology nodes. The overall CD variation budget in lithography can be separated into wafer mean, across wafer and across reticle field variation. In our paper we will concentrate on methods how to improve the across reticle CD variation. In a first section, we will compare scanner dose control and correction techniques with the Zeiss CDC technique done at reticle level. We will touch inherent challenges for both techniques in the logic application space where multiple different patterns have to be controlled accurately. The more the MEEF to dose sensitivity ratio matches for different features, the feature dependent correction becomes more accurate. We will discuss several applications from the 28nm and 22nm process node. Figure 1 shows this MEEF to dose sensitivity ratio out of S-Litho simulations for selected features for a 28nm metal application. As we can see, the deviations to a linear fit are acceptable and thus enabling a good correction for a wide variety of features. Please note that the features with negative dose sensitivity and MEEF are dark features whereas the others are bright features.

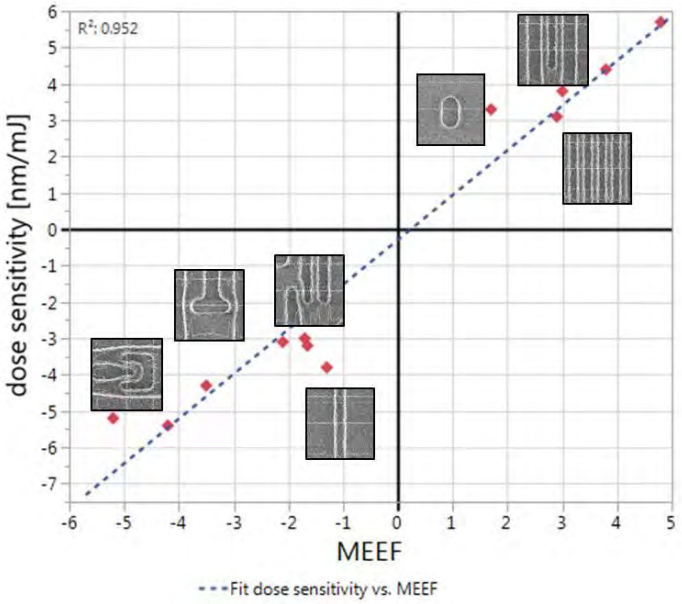



Figure 1. Dose sensitivity versus MEEF simulated for different features of a 28nm metal application.

In a second section we will discuss the CDC technique in more detail. This technique uses an ultra-short pulse laser technology, which generates a micro-level Shade-In-Element (also known as "Pixels") into the mask quartz bulk material. These pixels are used to selectively attenuate certain areas of the reticle in high resolution compared to any other method and thus excellent CDU improvements on reticle field level can be achieved. If we want to describe that principle in more detail, we need to consider both, the pure dose effect due to attenuation and the effect of the scattered light. A small part of that forward scattered light can enter the lens pupil thus creates some source blur. The amount of source blur is very small. However, in particular for illumination settings with extremely small pupil fill ratio, the impact on CD through pitch and on different patterning hotspots can be sensitive regarding the occurring source blur. The impact of the dose and the source part will be characterized based on measurements on scanner and wafer level. Further on wafer measurements are supported by simulations. With the help of specific scanner test masks that got different levels of CDC pixel density, both the impact on the illumination source and the dose transfer can be measured. To check the feature specific impact on the CDU correction, we show a correction of a “virtual” mask with an estimated CD-error of 2nm at mask level to be corrected. Figure 2 shows the on wafer CD deviation from target for 5 pitches for that mask, separated into three cases: the pre correction error (MEEF related), the dose-only correction (like we have at scanner dose correction) and the combined dose correction and source blur effect which occurs by using CDC correction. The result is somewhat surprising: The CDC sample with the combined effect shows a lower deviation for the 5 selected pitches than the pure dose based correction. This effect will be discussed in more detail.

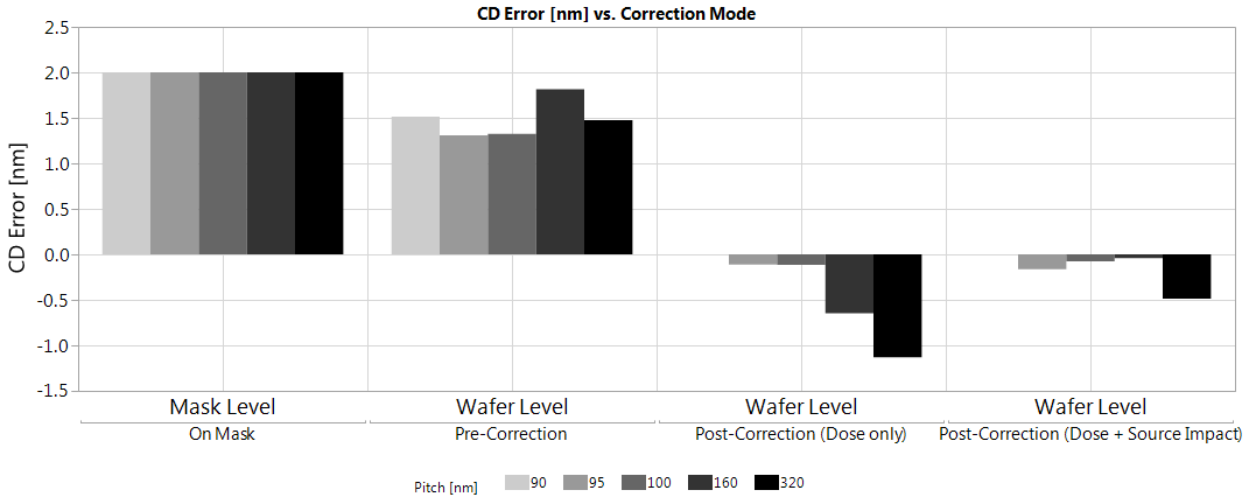



Figure 2. Simulated CD error at wafer level at an estimated 2nm mask error for different pitches. Comparison of pure dose correction result versus correction result including the combined dose and source effect.

Finally, we will discuss electrical verification results. For that experiment, two masks got programmed CD offsets on part of the reticle that resulted in a bad CDU. Afterwards, these masks got CDC treatment with the result of a “perfect” CDU. The CDC treated sample shows a significantly increased robustness of the product yield against disturbances as focus and dose variation. In a second step of that electrical verification test the CDC treated, originally “bad” masks are compared to two golden masks with inherently good CDU. No yield difference is observed. These results show that the CDC technique can be used to repair masks with a borderline CDU without any negative impact on patterning and yield.

**Keywords:** CDC, Critical Dimension Uniformity (CDU), simulation, yield, reticle, MEEF, hotspots

Abstract EMLC 2018

# PERFORMANCE VALIDATION OF MAPPER'S FLX-1200

Jonathan Pradelles[a,*], Yoann Blancquaert[a],, Stefan Landis[a], Laurent Pain[a], Guido Rademaker[a], Isabelle Servin[a], Guido de Boer[b], Pieter Brandt[b], Michel Dansberg[b], Remco Jager[b], Jerry Peijster[b], Erwin Slot[b], Stijn Steenbrink[b] and Marco Wieland[b]
*jonathan.pradelles@cea.fr

[a]*Univ. Grenoble Alpes, CEA, LETI, DTSI, Lithography Laboratory, F-38000 Grenoble, France*
[b]*MAPPER Lithography, Computerlaan 15 2628XK Delft, The Netherland*

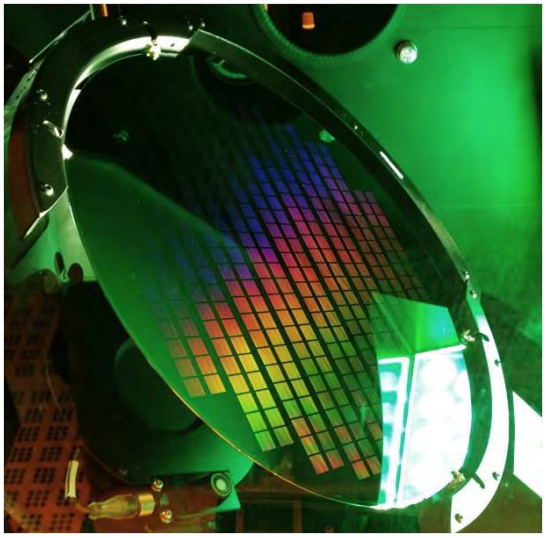
The launch of massively parallel mask less lithography is, without any doubt, an attractive solution for the semiconductor industry and opens new opportunity for the manufacturing of innovative chips. In partnership with MAPPER Lithography BV, CEA-Leti team assesses the progress of this technology and builds the full ecosystem required for its start-up in industry world.

Now Mapper production platform is on the path to industrial ramp-up. Mapper has installed its first operational product, the FLX–1200, at CEA-Leti in Grenoble (France). This is a maskless lithography system, based on massively parallel electron-beam writing with high-speed optical data transport for switching the electron beams. The FLX-1200, containing 65,000 parallel electron beams, has a 1 wph throughput at 300 mm wafers and is capable of patterning any resolution and any different type of structure all the way down to 28 nm node patterns. The system has an optical alignment system enabling mix-and-match with optical 193 nm immersion systems[1] using standard NVSM marks. The installation of this platform with the silicon Leti pilot line aims to develop quickly the process turnkey solution for specific applications : hardware encoded single chips for IoT market, low volume manufacturing, mastering.

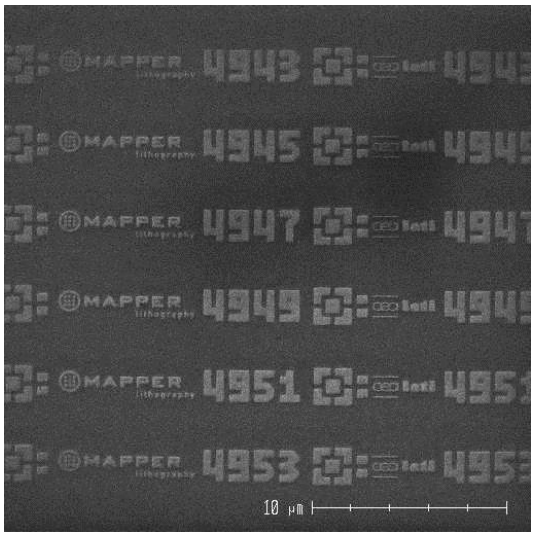
This talk will be focused on the presentation of the latest technical achievements of the FLX-1200. The main development item of this system has been the lifetime of blanker module that is the module that drives individually all the 65,000 beams. As of August 2017 the FLX-1200 has a fully operational electron optics column, including a 65,000 beam blanker. In August the first full wafer was exposed with this blanker, as shown in Figure 1. At the conference, we will report on endurance runs in full tool configuration and report on monitoring data regarding imaging. This talk will report as well on the latest overlay performances using standard image based overlay metrology as shown in Figure 2.

With the installation of its active blanker module, the Mapper production platform is now on its path to industrial ramp-up. This talk will also report on lithography demonstration examples of real devices printed on the FLX-1200 at Leti site

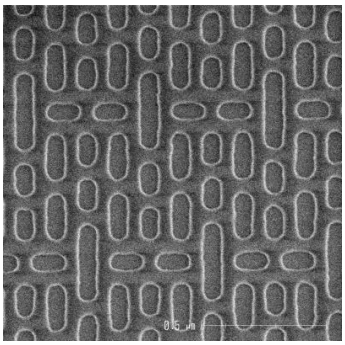
[1] N. Vergeer et al. "MAPPER Alignment sensor evaluation on Process Wafers", Proc. SPIE 8680, Alternative Lithographic Technologies V, 86801E



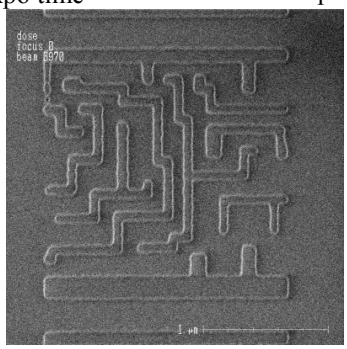
a 300mm wafer in 52min expo time



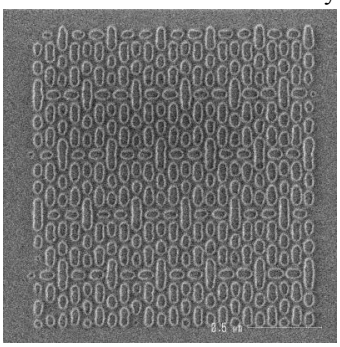

Beams operational and switch on/off individually



60 nm HP (N40)

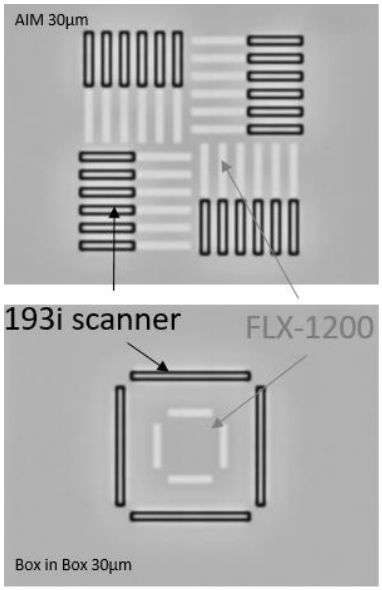



28nm Logic design



40 nm HP (sub N28)

Figure 1, First imaging results from the FLX-1200 at CEA-Leti with fully operational column and active blanker. All beam are driven individually



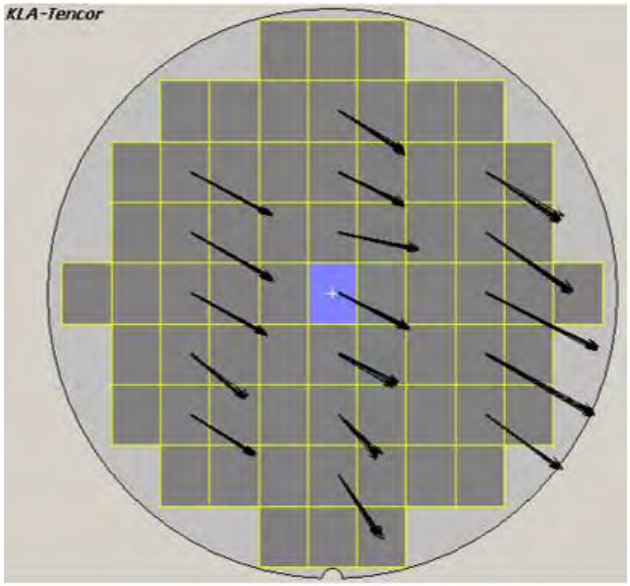




Figure 2, First overlay results from the FLX-1200 at CEA-Leti with respect to 193nm scanner and using standard image base overlay metrology.

Abstract EMLC 2018

# Feasibility of monitoring a multiple e-beam tool using scatterometry and machine learning: CD and stitching error detection

Guido Rademaker[a,b,*], Yoann Blancquaert[a], Thibault Labbaye[a], Lucie Mourier[a], Nivea Figueiro[c], Francisco Sanchez[c], Roy Koret[d], Jonathan Pradelles[a], Stefan Landis[a], Stephane Rey[a], Ronny Haupt[c], Barak Bringoltz[d], Michael Shifrin[d], Daniel Kandel[d], Avron Ger[d], Matthew Sendelbach[e], Shay Wolfling[d], Laurent Pain[a]

[a] *CEA, Leti, Minatec Campus, 17 Avenue des Martyrs, F-38054 CX 9 Grenoble, France*
[b] *Univ. Grenoble Alpes, F-38000 Grenoble, France*
[c] *Nova Measuring Instruments, GmbH, Moritzburger Weg 67 01109, Dresden, Germany*
[d] *Nova Measuring Instruments, LTD, P.O. Box 266, Weizmann Science Park, Rehovot 76100, Israel*
[e] *Nova Measuring Instruments, Inc., 3090 Oakmead Village Drive, Santa Clara, CA 95051, USA*

Direct-write electron beam lithography promises maskless patterning for mature to advanced nodes. This paper details the use of Nova's Optical Critical Dimension (OCD) tool for process control of a Mapper FLX-1200 multiple electron beam lithography system.

The FLX-1200 system exposes the substrate in raster scan mode by 65,000 beamlets, going through 1,352 lenses in groups of 49. Each group exposes a 2.2 µm-wide stripe along the field height.[1] This exposure strategy results in novel metrology challenges. Figure 1 shows a number of possible stripe-to-stripe variations due to dose and various registration errors: LCDU, *dx* and *dy* displacements and local magnification *Mx*. These variations enter the CD uniformity (CDU) and overlay (OVL) budget and need to be controlled.[2] Typical spectroscopic reflectometry targets are bigger than 2.2 µm, so the grating appears to be asymmetric and non-uniform inside the OCD spot, parting from the usual assumption of a perfect periodicity.

Non-periodic targets have been measured before by optical scatterometry, such as analysis of fingerprints and dislocations caused by the directed self-assembly (DSA).[3] In a previous work for multiple e-beam lithography, the treatment of targets with local (intra-grating) critical dimension uniformity (LCDU) errors in individual stripes have been addressed by measuring an effective CD.[4] This approach did not yet allow to distinguish between a uniform grating with a 'true' CD and a nominally non-uniform grating with identical 'effective' CD. Different approaches can potentially be used to make this distinction. For example, theoretical work on the reflectivity of gratings has shown that symmetry breaking can be probed using either the Mueller matrix methodology or spectroscopic reflectometry.[5,6] In this work, this distinction was investigated using machine learning algorithms, as well as through the use of additional scatterometry hardware channels of information.

We investigate the sensitivity of these techniques for different types of inhomogeneous gratings created by variable shaped beam (VSB) e-beam lithography to mimic various lithographic errors, for different stacks: Resist on silicon allows for ease of modeling and is interesting for tool monitoring and qualification, trilayer on silicon is the process of reference (POR), and allows for an etch transfer into silicon for higher optical index contrast.

Total Measurement Uncertainty (TMU) methodology is used to compare optical results to reference measurements by CD scanning electron microscopy (CD-SEM) and atomic force microscopy (AFM).[4] Results for effective CD are shown in figure 2(a), while spectra using the additional hardware channels to detect non-uniformity are shown in figure 2(b). Preliminary results with machine learning of gratings in trilayer with *dx* stitching errors are shown in figure 3.

**Keywords:** machine learning, optical critical dimension, multiple electron beam lithography, maskless lithography, stitching, TMU, Total Measurement Uncertainty, Spectroscopic reflectometry

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2. P. Brandt et al., "Alternative stitching method for massively parallel e-beam lithography," J. MicroNanolithography MEMS MOEMS **14**(3), 031203 (2015) [doi:10.1117/1.JMM.14.3.031203].

* Corresponding author: guido.rademaker@cea.fr

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4. Y. Blancquaert et al., "Scatterometry control for multiple electron beam lithography," in Proceedings of the SPIE **10145**, pp. 101451F-101451F – 12 (2017) [doi:10.1117/12.2261389].
5. L. Li, "Symmetries of cross-polarization diffraction coefficients of gratings," JOSA A **17**(5), 881–887 (2000) [doi:10.1364/JOSAA.17.000881].
6. D. Shafir et al., "Mueller matrix characterization using spectral reflectometry," in Proceedings of the SPIE **8789**, pp. 878903-878903–878909 (2013) [doi:10.1117/12.2022549].

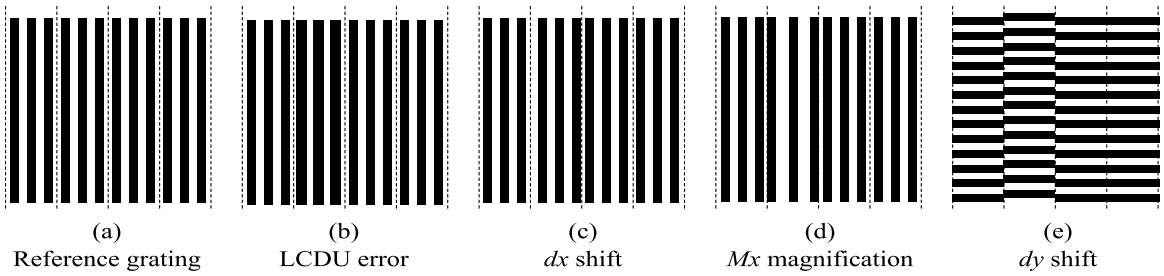


FIG. 1. Mapper exposes 2 µm-wide zones called stripes. The following grating types have been exposed: (a) Reference grating (b) Local critical dimension uniformity (LCDU) error due to dose modulation. (c) Pattern shift *dx*. (d) Magnification in *x* due to electron beam deflection strength. (e) Pattern shift *dy* in one stripe.

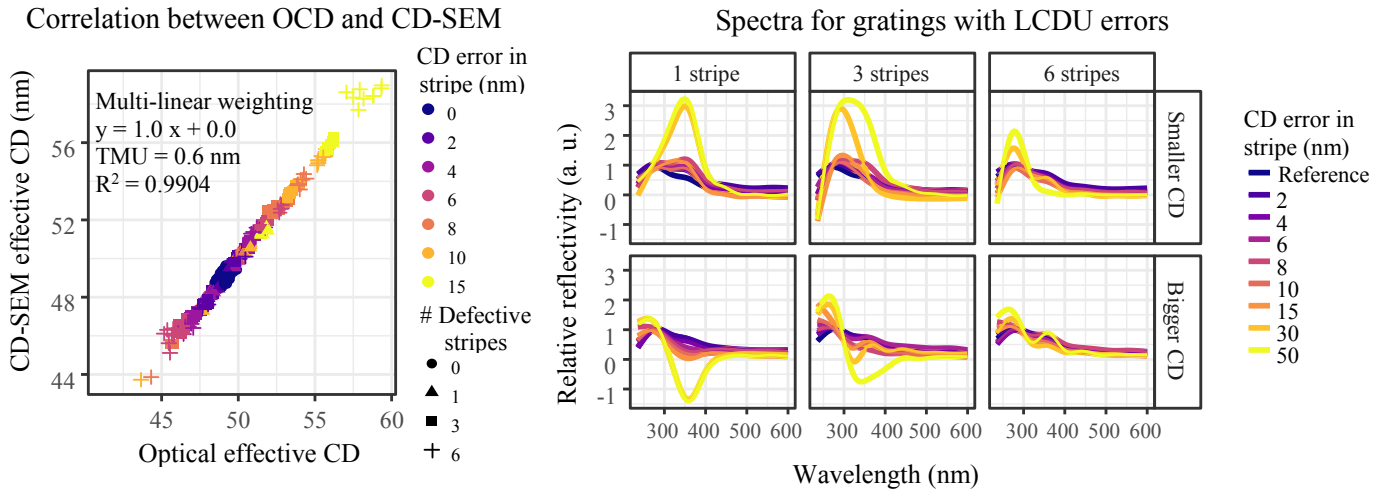


FIG. 2. (a) OCD measurements on targets with 1-6 stripes with LCDU error show a very good correlation to multi-linearly weighted CD-SEM reference for effective CD for resist on silicon. (b) Spectra from portions of the full wavelength range using additional hardware channels show a clear distinction between uniform (reference) targets and targets having stripes with an error in CD.

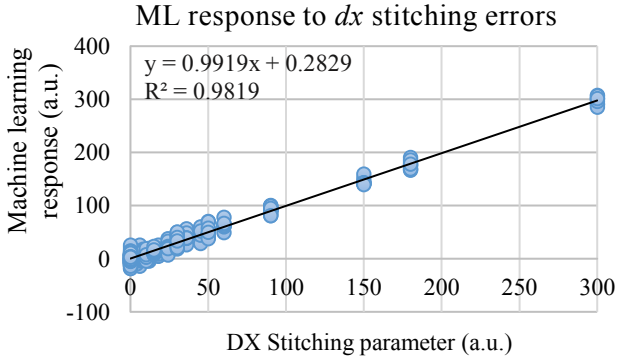


FIG. 3. Preliminary results of machine learning on *dx* shifts, showing a good correlation to programmed error.

# Wafer-Level UV-Nanoimprint Lithography for high resolution and complex 3D Structures

Thomas Glinsner, Martin Eibelhuber, Georg Berger, Mustapha Chouiki
EV Group, St. Florian am Inn, 4782, Austria

Claudia Lenk, Martin Hofmann, Steve Lenk, Tzvetan Ivanov, and Ivo W. Rangelow
TU Ilmenau, MNES, IMNE, Gustav-Kirchhoff-Straße 1, 98693 Ilmenau, Deutschland

Ahmad Ahmad, Alexander Reum and Mathias Holz,
Nanoanalytik GmbH, Ehrenbergstr. 1, 98693 Ilmenau, Deutschland

E-mail: **t.glinsner@evgroup.com**

Nanoimprint lithography (NIL) is a high-throughput and scalable lithography technique which has entered into industrial volume manufacturing. In particular, NIL offers a cost-effective and scalable process for replicating of complex 3-dimensional (3D) patterns onto a wide selection of substrates. Applications for such nanometer and micrometer scale, precisely manufactured 3D structures include diffractive and refractive optical elements, other optical or photonics components, data communications, augmented/virtual reality (AR/VR), security features, biotechnology and nanofluidics to name just a few.
In the frame of the European project SNM (Single Nanometer Manufacturing for beyond CMOS devices) manufacturing techniques for next generation devices demanding smallest feature sizes have been investigated. In this work we will review the final status of the obtained results using nanoimprint lithography for high resolution nanopatterning of single electron transistors (SET) and more complex structures like holographic features, blazed gratings and multi-level gratings. The structures were fabricated by direct writing using field-emission scanning probe lithography, thermal scanning probe lithography, imprinting and etching. Although these mask-less methods like field-emission scanning probe lithography (figure 2) can already provide the requested resolution quality of the nanopatterns, they lack in writing speed and large area manufacturing capability and thus in throughput demands required for industrial device manufacturing. However, these methods can be perfectly combined with NIL to master the strength of both approaches. NIL enables the replication of high resolution features on large areas and provides high throughput, but it requires supporting technologies for the patterning of stamps which is covered with these direct writing technologies. EVG´s SmartNIL™ is a UV-based imprint technology employing polymer working stamps to transfer high resolution, 3D complex structures in a conformal imprinting approach at wafer level in a single process step. The integration of the SmartNIL™ technology into a fully integrated tool platform called Hercules covers the whole imprinting process chain combining pre-processing steps like cleaning, spin coating and baking with NIL (figure 1). The layout of the SET devices includes high resolution patterns with a distance between the channels of less than 50 nm and the according master for the nanoimprint process were chips with a size of 1.5 x 1.5 $cm^2$. For the definition of the layout a mix & match approach was applied. In this context, contact pads as well as an active area for FE-SPL patterning were fabricated by optical lithography & standard reactive ion etching. As a result the master consisted of elevated patterns at the contact pads with a height of approx. 25-28 nm and small trenches with a depth of approx. 15 nm compared to the surrounding. This master was replicated to a polymer working stamp which was then used for patterning of silicon wafers by using the SmartNIL™ technology. The structures replicated by the described process and according AFM measurements of the master and imprint are depicted in figure 3. Subsequently the structures have been etched into the silicon substrate, proving high fidelity pattern transfer into the substrate as can be seen in figure 4.

**Figure 1:** Hercules NIL system for fully automated SmartNIL™ nanoimprinting including pre-processing modules.

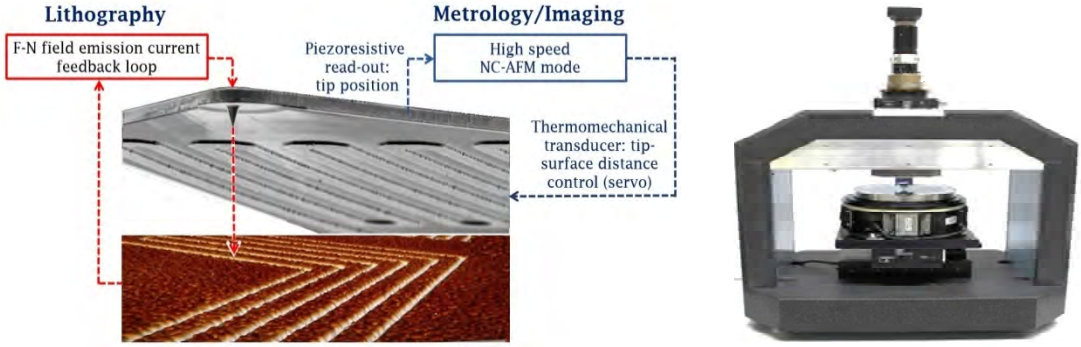


**Figure 2:** a) Principle of the electron Field-Emission Scanning Probe Lithography system (FE-SPL) based on so called active-cantilever (self-sensing and self-actuating cantilever). b) FE-SPL tool used for the fabrication of the templates and capable for SPL "step and repeat" on 150mm wafer.

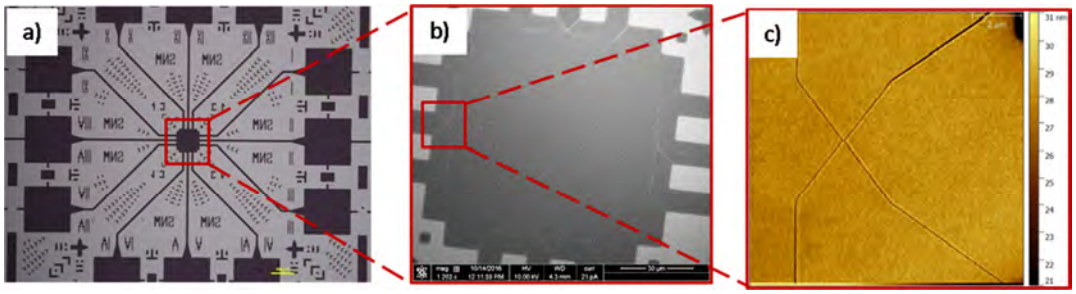


**Figure 3:** a) Optical image of one field of the SET layout including contact pads (black). b) SEM image of middle field marked in (a). c) AFM image of SET pattern marked in (b).

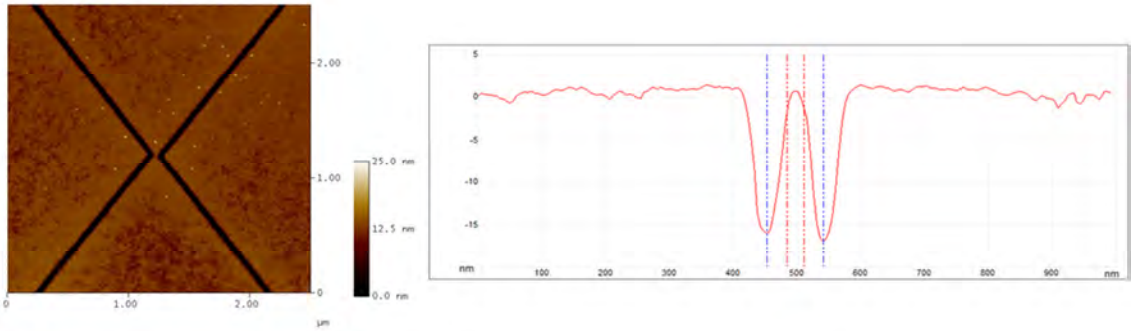

**Figure 3:** AFM image profile (through the channel) after etching using an optimized sequence for plasma descum, $SiO_2$ breakthrough and Si etch.

**100-word text summary**

Through their joint program INSPIRE, EVG and CEA-LETI demonstrate the benefits of the wafer scale NIL technology, its integration capabilities and spread its use for applications beyond semiconductors. This paper presents the rules-based corrections strategy and dedicated qualification masters developed and manufactured by LETI in order to assess the performances of nanoimprint process. The master are manufactured in silicon substrates with DUV ASM300 lithograhy and present 1600 various design that are replicated with the SmartNIL™ technology available on the HERCULES®NIL equipment platform. The work brings focus on sub-micrometer resolution features with variable pitch, CD and density. CDU measurements are performed on masters and imprints on dedicated features, and comparisons are made to estimate the bias tables between the original layout, the master and the replicas. Finally the correction strategies are discussed in terms of relevance and reliability, we underline the specific needs for nanoimprint: feature type and feature position dependent corrections.

**500-word text abstract**

# Application of rules-based corrections for wafer scale nanoimprint processes and evaluation of predictive models

H. Teyssedre*[a], P.. Quemere[a], J. Chartoire[a], F. Delachat[a,b], F. Boudaa[a], L. Perraud[a], M. May[a]

[a]CEA-LETI, Minatec Campus, 17 rue des martyrs Grenoble, 38054 Cedex 9, France;
[b]INTITEK, 20 Boulevard Eugène Deruelle 69003 Lyon, France
*corresponding author: hubert.teyssedre@cea.fr

NanoImprint techniques stick out from other more conventional lithography processes (photolithography, electronic lithography, EUV lithography) by virtue of the fundamental mechanisms that create the structures. With conventional approaches the structures are created through a chemical contrast, whereas a topographic one is formed in the case of NanoImprint thanks to the flow of the resist through the stamp's cavities.

In twenty years, consequent technical developments have been achieved to make the technology more mature. Among a plenty of technology alternatives, the UV-based imprint, using transparent stamp, became the standard technology. Two well established options are now available on the market: the full wafer imprint (the size of the stamp correspond to the size of the wafer to be printed) and the step and flash imprint were a small stamp (i.e. die size) is stepped across the wafer to be processed.

If the step and flash technology has demonstrated its capabilities to address the semiconductor markets with high-requirement levels for alignment capability and defectivity density, the full wafer option seems to be the reference for the emerging and growing markets like LED and Photonics based devices having lower defectivity level requirements. To fulfill the market needs,

some items of the supply chain such as master manufacturing and design rules need to be qualified to support the development of new applications.

Within that scope, CEA-Leti and EV Group investigated the Critical Dimension Uniformity evolution along the imprint process with the SmartNIL™ technology to establish design rules and rules-based corrections strategies for the replication process. Based on our knowledge and advanced tools used for layout correction and optimization, we assess the well-known line-space corrections, their limitations and the required evolutions in term of computing that will be mandatory to obtain mature and relevant 'nanoimprint ready' masters.

In this paper, we present the dedicated masters developed and manufactured by LETI in order to assess the CDU, defectivity and overlay performances of the SmartNIL™ process within the same design. The master are manufactured in silicon substrates with DUV ASM300 lithograhy and present 1600 various design, presented in figure 1, that includes line-space patterns, dots, contacts and squares with square and hexagonal arrangements. Around 80 designs were characterized to build the bias table, as presented in figure 2 for the imprint. The critical dimensions range from 250 nm to few micrometers and etched depths from 140 nm to 1 µm. The masters are prepared and replicated with a process of reference (EVG/AS1 for the working stamps and EVG/UVA for the imprint resist) on the Hercules platform. CDU measurements are performed on masters and imprints on the selected features, and comparisons are made to estimate the bias, as illustrated in figure 3 for the pitch, between the original layout, the master and the replicas. Interpolation of the measurements are discussed to underline the specific needs for nanoimprint: feature type and feature position dependent corrections. Finally the corrections tables are applied to tests features to validate the relevance and reliability of the corrections.

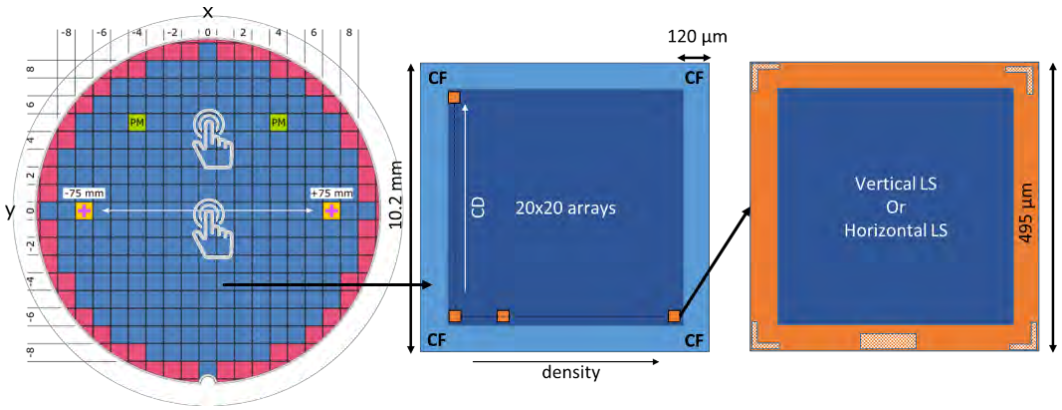


Figure 1: Silicon masters mapping (256 cells, each containing 400 arrays of periodic lines and spaces) used for the CD uniformity assessment. The cells are 10.2x10.2 mm. The pattern density (line CD/pitch) in the arrays ranges from 0.1 to 0.9 for CD ranging from 250 to 3500 nm, each design in horizontal and vertical orientations. Each array is 395x395 µm surrounded by a

periphery of dummy patterns of a density close to the arrays to reach a good imprint uniformity. The cells measured by CDSEM are cells (0,0) and (0,5) highlighted by the fingers.

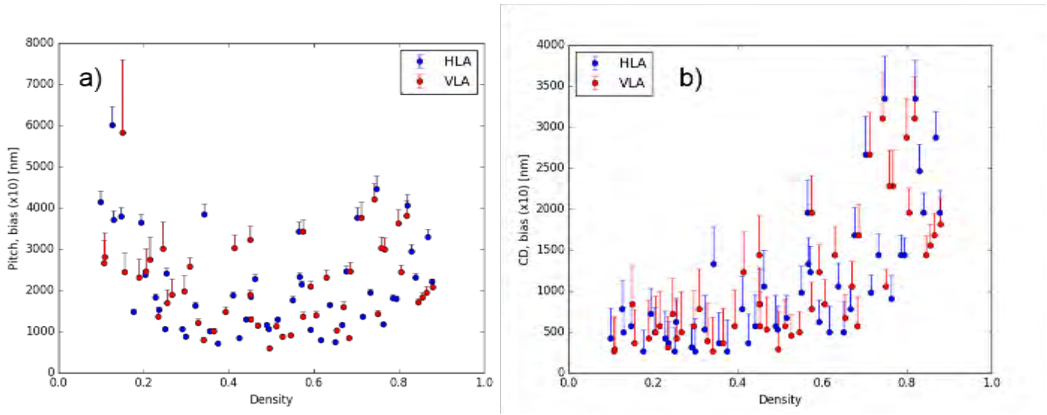


Figure 1: Target values and bias for the imprints for the pitch (a) and the CD (b). A signature is observed on low density patterns. For the pitch, the error bars show significant increases of the bias for all the targets above 2 µm compared to the master, with a particular impact on the vertical lines (red) for densities between 0.1 and 0.3. For the CD, the influence of the feature orientation is not significant.

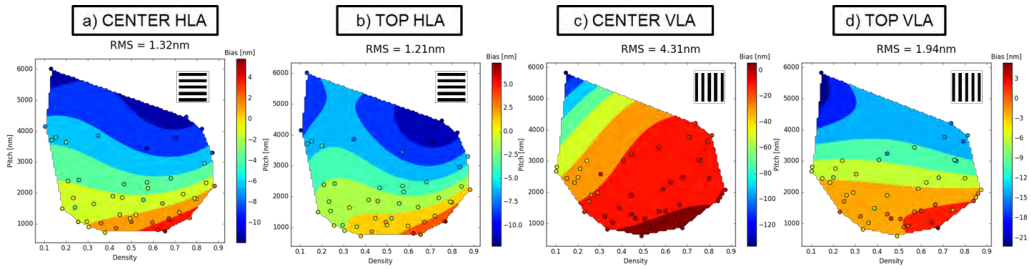


Figure 2: Pitch - Difference between the master pitch and the imprint pitch for the vertical and horizontal lines, at the cell in the center of the wafer (0,0) and at the top of the wafer (0,5). A significant change on the signature and on the range of the bias (from -130 to 5 nm) is captured with the case (c) and reveal the influence of the pattern orientation (either horizontal or vertical) by comparison with case (a), and the influence of location on the wafer with comparison to case (d).

# Silicon nanowires patterning using UV-assisted graphoepitaxy DSA lithography

M. Argoud[a], G. Claveau[a], P. Pimenta Barros[a], Z. Chalupa[a], G. Chamiot-Maitral[a], C. Navarro[b], C. Nicolet[b], I. Cayrefourcq[c], R. Tiron[a]
[a]CEA-LETI, MINATEC Campus, 17 Rue des Martyrs, 38054 Grenoble, France
[b]ARKEMA FRANCE, Route Nationale 117, BP34 - 64170 Lacq, France
[c]ARKEMA FRANCE, 420 rue d'Estienne d'Orves, 92705 Colombes, France

**Keywords**: Directed Self-Assembly, Block-Copolymers, Graphoepitaxy, Line/Space Patterning, Surface affinity, UV modification, Silicon Nanowires

Directed Self-Assembly (DSA) of block-copolymers, which is an affordable, simple and versatile lithography technique, is still highly investigated as a potential solution for the next generation node in the CMOS industry. DSA graphoepitaxy approach provides physical confinement between two "sidewalls" of fixed surface energy, which will generate well defined line/space structures with a variety of block copolymer materials and process environment [1,2,3]. However, most pilot-line compatible processes found in literature use Electron Beam Lithography (EBL) to generate the guiding structures because non-preferential grafted polymer layers can be incorporated between the HSQ resist (oxide guiding templates) and an inorganic transfer layer [4]. When using a 193nm-immersion lithography, such integration flow is not advised because the 193nm resists are acrylate-based resists that flow during the different annealing steps (CD uniformity and roughness performances impacted). Guiding templates made of standard immersion "hardmask" stack material with proper surface functionalization (sidewalls attractive to one block, bottom non-preferential) are rare.

This work presents a smart surface modification technique for precise control over the surface affinity of topographic gratings used for the 300mm graphoepitaxy of PS-*b*-PMMA lamellar block copolymer (figure1). Guiding template manufactured for DSA of BCP is herein compatible with conventional 193nm dry lithography using standard SiARC/SOC materials stack. The method uses the property of various copolymers brushes to undergo UV-induced oxidation. Coupled with simulated intensity profiles inside a 3D grating structure, we present a way to precisely select the free surface energy distribution inside the grating. In this work, both homo-polystyrene and PS-*r*-PMMA thin films grafted to the surface of the grating are modified. The result is non-preferential wetting promoted at the bottom interface while sidewalls are left highly PMMA attractive. Topographic gratings for DSA combined with such UV-modification technique provides tremendous versatility in the final assembly and design of PS-*b*-PMMA line/space features.

This specific DSA process was implemented on the 300mm pilot line at Leti, and incorporated in a process flow for the creation of nanowires-like transistor as depicted in figure 2. Single crystalline silicon nanowires patterning on $SiO_2$ layer (from SOI substrate), achieved after the last Si etching step of the cut level, is especially highlighted (figure 3). The PS lamellae are also used as a mask through several etching steps to produce *in fine* high aspect-ratio structures inside silicon (figure 4). Different PS treatment (e-beam, UV or plasma curing) before etching transfer are moreover investigated in order to improve the final line roughness of Si fins. The best etching strategy will be selected based on the LWR-3σ and PSD studies done at each critical steps of the integration flow. As perspectives, the integration flow presented in this paper will be employed for patterning Si/SiGe nanowires.

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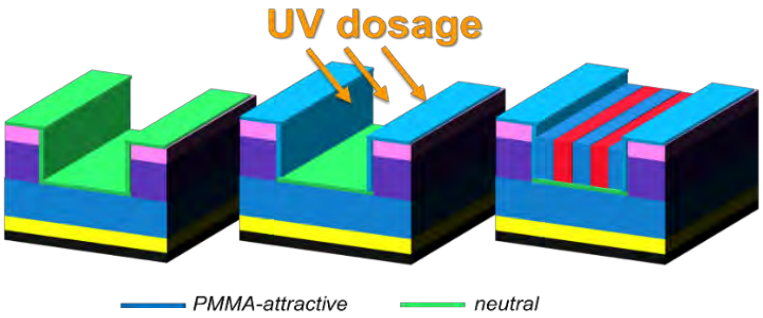
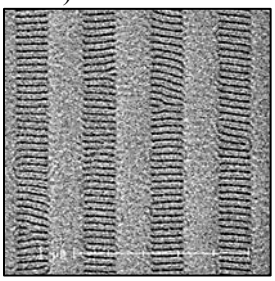
[2] Tsai, H. et al, two-dimensional pattern formation using graphoepitaxy of PS-b-PMMA block copolymers for advanced Finfet Device and circuit fabrication. ACS Nano 2014, 5(5), pp 5227-5232
[3] Girardot, C. et al. Pulsed Transfer Etching of PS−PDMS Block Copolymers Self-Assembled in 193 nm Lithography Stacks. ACS applied materials & interfaces 2014, 6, 16276-16282
[4] Tsai, H.-Y. et al. Sub-30 nm pitch line-space patterning of semiconductor and dielectric materials using directed self-assembly. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures 30, 06F205 (2012)

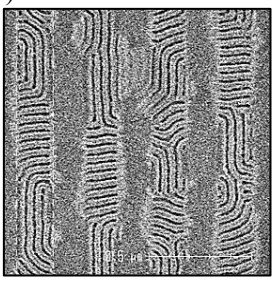
a) UV-assisted graphoepitaxy




b) Without UV



c) Intermediate UV dose



d) Strong UV dose

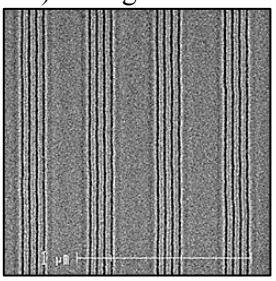
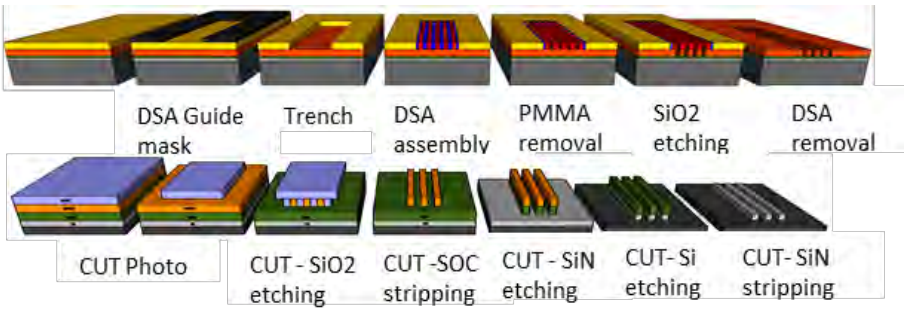


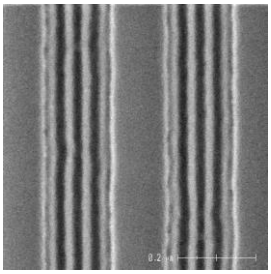
Figure 1: a) Principle of UV-assisted graphoepitaxy approach that consists in grafting a PS-*r*-PMMA layer and then exposing the pattern sidewall to UV exposure. b), c), d) Top-view CDSEM image after DSA without UV exposure, an intermediate UV dose and strong UV dose, respectively.

a)

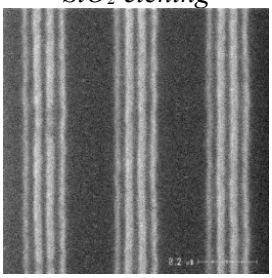



b)

*PMMA removal*



*$SiO_2$ etching*



*Si etching*

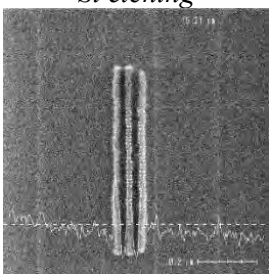


Figure 2: a) The DSA integration flow used to pattern silicon nanowires on SOI substrate b) Top-view CDSEM image after PMMA removal, $SiO_2$ and final Si etching with the cut level.

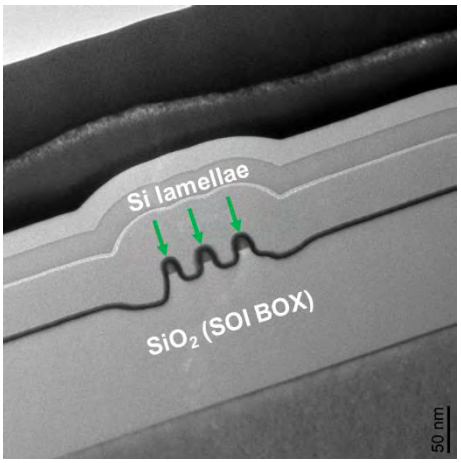
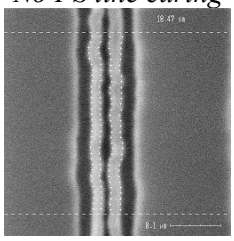


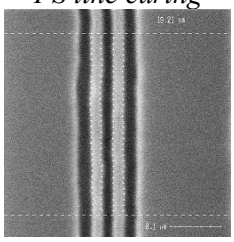

Figure 3: Cross-sectional TEM image of a 3-active Si fins achieved after the last Si etching step of the cut level.

a)

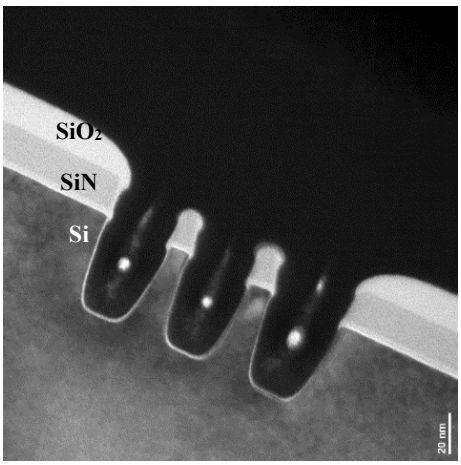
*No PS line curing*



*PS line curing*



b)




*Si fin depth ~45nm*
*Si fin width ~10nm*

Figure 4: a) Top-view CDSEM image after Si etching without and with PS line curing b) TEM image after Si etching showing two fins with a height of 45nm and a width of 10nm.

# Alternative absorber materials for mitigation of mask 3D effects in high NA EUV lithography

F.J. Timmermans, J. Finders, J. Mcnamara, E. van Setten

ASML Netherlands B.V., De Run 6501, 5504 DR Veldhoven, The Netherlands

EUV Lithography (EUVL) enters the phase of high volume manufacturing of integrated circuits. The EUV photomask is a key aspect in achieving a high quality imaging capability. This makes a fundamental understanding of mask properties and their impact on the aerial image essential.[1] One of the challenges for EUV masks that needs to be addressed are the mask 3D (M3D) effects. Understanding of M3D effect on imaging, and mitigation strategies such as implementation of thinner high-k absorber stacks remains critical for the upcoming high-NA EUV scanners. The combination with high NA, anamorphic imaging, and the central obscuration needs to be considered.

M3D effects are caused by the high mask topography (relative to the actinic wavelength), the oblique incidence angle on the reticle, and the multilayer reflectivity, see figure 1.[2] This affects the pattern shift through varying sigma of the source pupil, which results in contrast fading of the image. The limitation on image performance from M3D effects will reduce the available process window and increase local CDU (LCDU) imaging defects. Several mitigation strategies exist to recover this contrast such as source mask optimization.[3] Additionally the anamorphic design on high-NA systems reduces the reticle incidence angle in the scanning direction. This significantly reduces M3D effects for horizonal features, while increasing these effects in the vertical direction by the increase in NA. In this work the implementation of an alternative absorber material is investigated for the reduction of mask aberrations specifically for high-NA.

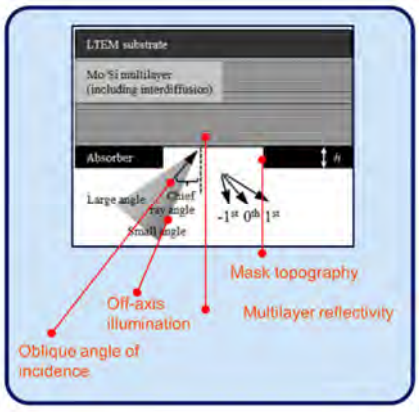



Figure 1: Schematic reticle topography and oblique light incidence.[2]

Alternative absorber materials with a higher extinction coefficient or k-value allow for thinner absorber stacks to be used, and may reduce contrast fading and pattern shifts. An investigation of such materials requires several parameters to be taken into account. First the material thickness and n&k values directly impact imaging performance. Additionally a change in the mask will likely require a new optimization of the source pupil for ideal imaging performance. These subjects are also critical for a possible high-Na scanner where they are considered in

conjunction with the use of high-NA and anamorphic imaging. In figure 2 simulations of the contrast (NILS) and dose for a point source scanned through the pupil sigma-x and sigma-y are shown for the example structure of regular contact holes (CHs) with CD 11nm and pitch 22nm. The currently proposed absorber stack Tantalum 55nm thick is compared with a high-k Nickel 33nm thick absorber. For the Ni33 absorber an increase in NILS is observed, this increase is highest in the x-direction. This can be expected, due to the anamorphic system the x-direction is the most critical as a result of the larger M3D effects this is where the high-k absorber provides the largest benefit. However also a higher dose to print is found for the nickel absorber, indicating a lower reticle reflectivity. It is also found that the nickel absorber may enable to use a much larger area of the source pupil because a high contrast is achieved for a larger range of source points. The potential larger pupil fill ratio (PFR) may result in an optical throughput gain for systems with a PFR limit without transmission loss of ~20%. Impact of the central obscuration is seen in the dark ring in the center and at the left and right sides of the NILS-x pupils, here one of the diffracted orders of light is blocked.

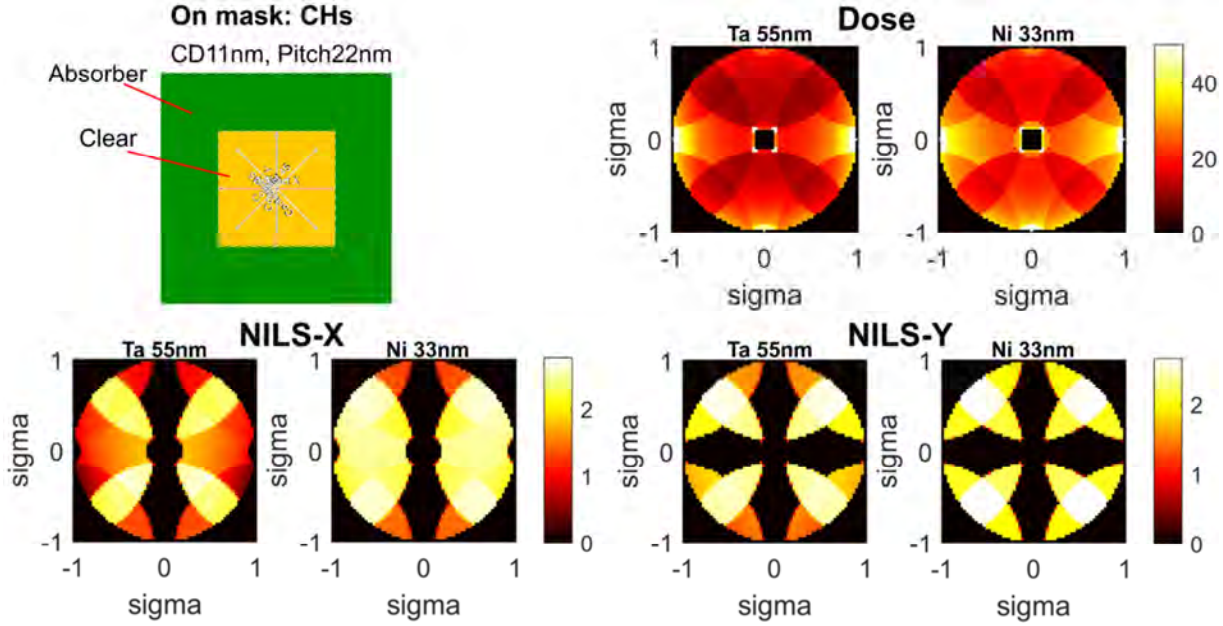



Figure 2: Comparison of Ta55 and Ni33 absorbers for CHs with CD11 Pitch22. Imaging performance for both absorbers through the source pupil is analyzed for NILS in X and Y direction, and the required dose to print.

A comparison of multiple absorber stack configurations for various high-NA scanner use cases will enable a better understanding of the absorber impact on imaging, and the specific differences of this impact in comparison with 0.33 NA EUVL systems. Imaging metrics of interest are among others: contrast, dose to print, DOF, exposure latitude, and MEF. It is expected that the absorber change while improving most imaging metrics may result in a degradation of some other imaging parameters. The challenge is in weighing all effects to determine the optimum performance. Multiple materials with various n&k values are of interest, resulting in a large parameter range of which the influence on imaging needs to be investigated. Figure 3 presents the performance comparison between two high-k absorbers that have been identified as potential alternative materials[4,5] (Cobalt 33nm and Nickel 33nm) and the current Tantalum 55nm. The same regular CHs pattern CD11P22 is used, with a standard quadrupole illumination source. The following imaging metrics are compared: dose to print,

NILS (X and Y direction), LCDU, mask error factor (MEF), pattern shift (PS), non-telecentricity (nonTEL), and exposure latitude (EL). As LCDU metric the NILS^2/dose is used, to indicate how LCDU changes for contrast and dose to print. Overall an improvement in performance is seen, specifically the higher NILS and decreased nonTEL and EL gives an indication that the through focus performance will increase with the alternative absorbers. The impact on NILS and nonTEL is in agreement with previous computational lithography studies to line spaces on high-NA.[6] Other studies have also show an increased DOF and reduced nonTEL for high-k absorbers with high-NA EUVL.[7] An investigation for further use cases will be used to find the performance comparison with current 0.33 NA EUVL systems. Additionally other potential absorber materials may give further insight in what optimal stack configurations can be obtained.

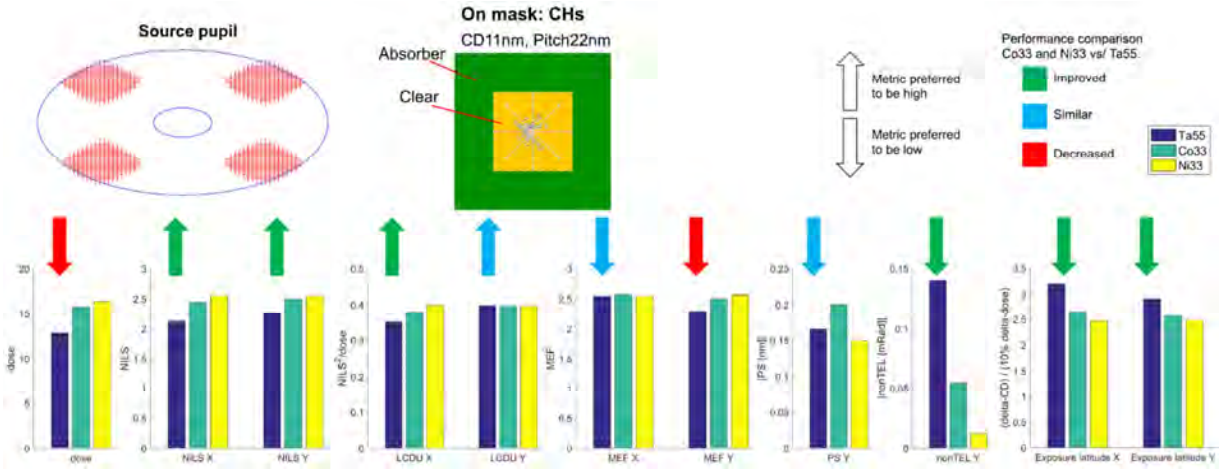



Figure 3: Comparison between three different absorber stacks the currently proposed Tantalum 55nm, and two commonly named high-k absorber materials Cobalt 33nm and Nickel 33nm. As use case the regular contact hole with a standard quadrupole source is used. The bar graphs report on the comparison for various imaging metrics: dose, NILS, LCDU, mask error factor, pattern shift, non telecentricity, and exposure latitude. The arrows and their colors indicate the preference of the metric to be high or low, and the relative performance of the high-k vs. the Ta55 absorber.

[1] Laurens de Winter et al., SPIE European Mask and Lithography, 2015
[2] Thorsten Last et al., SPIE Photomask Technology, 2016
[3] Jo finders et al., SPIE Extreme Ultraviolet Lithography, 2017
[4] Vicky Philipsen et al., Proc. of SPIE Vol. 10143 1014310-1, 2017
[5] Vicky Philipsen et al., Proc. of SPIE Vol. 10450, 2017
[6] Eelco van Setten et al., Proc. of SPIE Vol. 10450 104500W-1, 2017
[7] Weimin Gao., Proc. of SPIE Vol. 10583 10583O-1, 2018

# Advances in multi-layer deposition of EUV mask blanks: Current status and roadmap

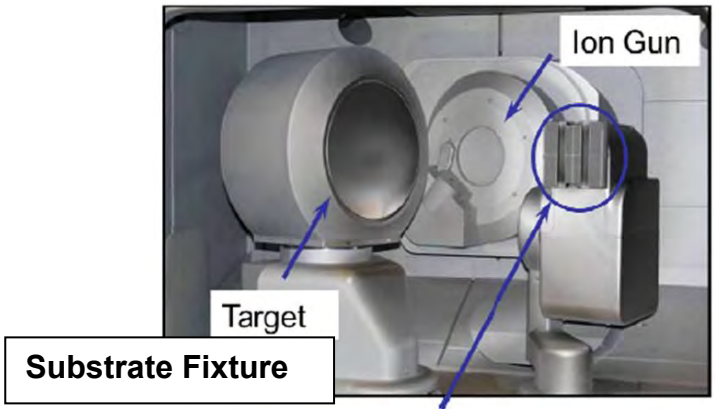
Katrina Rook, Sandeep Kohli, Meng Lee, Boris Druz,

Frank Cerio, Adrian Devasahayam

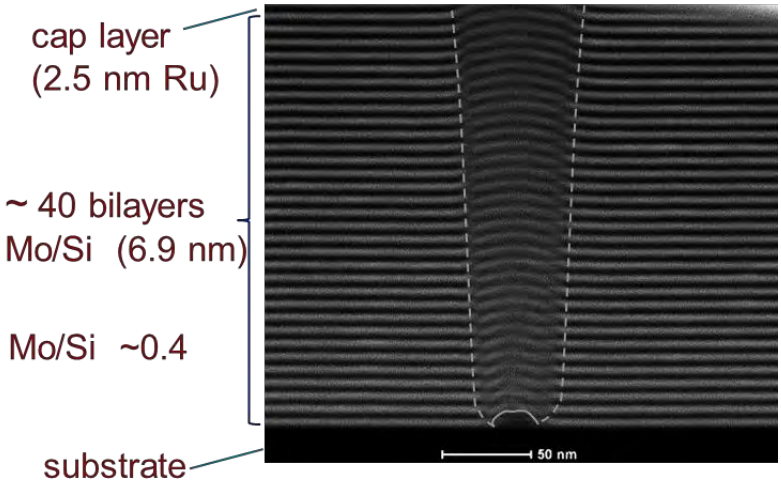
## Abstract

Developments extreme ultra-violet (EUV) technology over last few decades has brought us to a point where application of extreme ultra-violet (EUV) lithography for 7 nm and lower process nodes is very near possibility. Deposited multilayers of molybdenum (Mo)/ silicon (Si) on glass substrates are used to create EUV mask blanks that are a key component of high-volume manufacturing (HVM). In keeping the pace with the needs of EUV market, the deposition processes for Mo/Si have evolved significantly. While the technical risks of defects for the mask blank are much lower at this time, more advances are needed to improve yield from these masks, have better process control and further improve defects as applications of EUV lithography are further challenged (example multiple patterning). Further technical improvements are needed to follow the existing HVM ramp while keeping improvements from the past.

In this presentation, we will present some of the recent improvements for the mask blank manufacturing using Veeco NEXUS IBD-LDD Ion Beam Deposition System. For example recent technical and handling improvements have led to production of significant number of 0-defect masks at > 54 nm [1] and a beam over spray reduction of > 50 x [2]. We will also present technical roadmap for improvements in the mask manufacturing to further improve defect levels, yields and throughput to enable HVM ramp. Some new ideas and platforms will be introduced for this.




Ion Beam Low Defect Deposition System




Cross-section of EUV mask blank coating with particle defect

References:

[1] Antohe et al.; Proceedings of the SPIE, Volume 9048, id. 90480H 8 pp. (2014).

[2] Devasahayam et al; Proceedings of International Workshop on EUV Lithography, June 12-15, 2017, CXRO, LBNL , Berkeley, CA (2017)

# Revival of grayscale technique in power semiconductor processing under low-cost manufacturing constrains

Jens Schneider, Dieter Kaiser, Nicolo Morgana, Henning Feick
Infineon Technologies Dresden GmbH Koenigsbruecker Strasse 180, 01099 Dresden Germany

## ABSTRACT

Grayscale lithography is a well-known technique for three dimensional structuring of a photo sensitive material. The 3D structuring of the photoresist is performed by a spatially variable exposure. Pixelated grayscale mask structures are defined to achieve the desired 3D resist patterns by locally variable transmittance values. Within power semiconductor processing, grayscale techniques could beneficially be applied in different process steps. Several ideas come to mind for process simplification, alternative integration scheme and more, e.g. the realization of 3D resist patterns for implant applications in order to control the doping depth and profiles and their influence on device parameters. In order to make the grayscale process useful for manufacturing of semiconductor devices it is necessary to master and consider the inherent process variability. Lithographic simulation is used to optimize the sub-resolution photo-mask features and to predict the final resist shape and its variability. Device simulation for a 32V DMOS device, used in our 130nm technology node, shows that the device performance would benefit from an attenuation of the implant dose in the center of the device, which could be achieved by creating a resist island with reduced resist thickness in the center of the drawn implant opening of the DMOS device. In order to achieve the desired target geometry of the implant resist mask, simulations with Sentaurus Lithography have been performed resulting in a suitable mask design and lithographic process. We will demonstrate the development of the grayscale litho-process based on the needs of an implant scheme that is going to be used for a 32V DMOS device, with respect to process stability and achieved resist mask dimensions.

## 1. INTRODUCTION

Most of the lithographic layers of our technologies are used for implant applications with different resist materials and film thicknesses. One disadvantage of the state of the art process are the subsequent high temperature steps, very often combined with wafer warpage issues and non-correctable overlay errors and the imprecise definition of doping area and depth with impact on the device stability. In a nutshell the state of the art implant process allows only limited device architectures and is characterized by an increased process complexity. We follow an idea to use 3D lithography structures defined by grayscale lithography for a spatial patterning of the implant depth. [1]
To achieve the appropriate doping profile, the drift region of a power MOSFET is fabricated using several implantation sequences, resulting in the usage more than one implant mask. In order to achieve the desired device performance the target of our work is to create a 3d resist structure with reduced resist thickness in the center of the drawn implant opening of a NLDMOS device. The demanded resist dimension are shown below, the reduced thickness target is 900nm and the gap of the island to the main feature should be 600nm, with a standard resist thickness of 3µm.

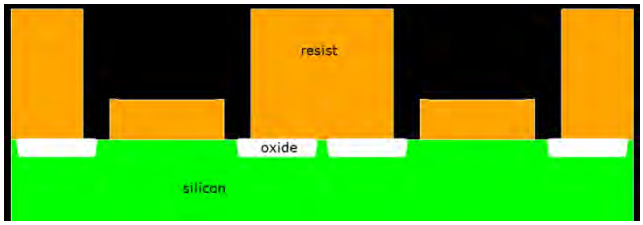
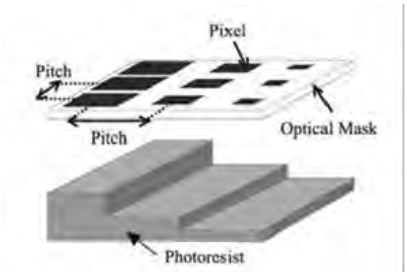



Figure 1. target resist structure for deep p-body implant of 32V DMOS device

## 2. EXPERIMENTAL SETUP AND METHODOLOGY

For our grayscale process we used a photomask with pixilated sub-resolution features of different sizes and pitches to locally modulate the intensity of the applied UV light. The amplitude of the intensity depends on the sub-resolution pixel

size, their arrangement and pitch on the mask. For a given dose these areas will develop to different resist thicknesses according to the different amplitudes of intensity.



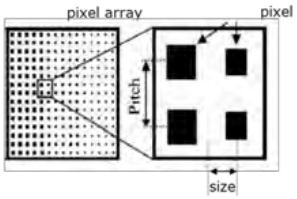




Figure 2. pixilated sub-resolution features for grayscale process

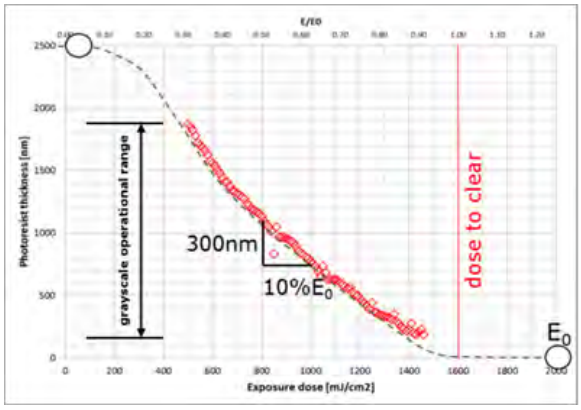



Figure 3. measured i-line resist thickness as function of exposure dose

The grayscale process is done using a standard i-line resist with 3µm thickness on a Canon iZ stepper, which offers an improved dose uniformity compared to Canon i5 steppers. In order to create a test mask for evaluation of suitable patterns and process window, simulations with Sentaurus SLitho (2017-6) have been performed with a calibrated resist model.

## 3. RESULTS

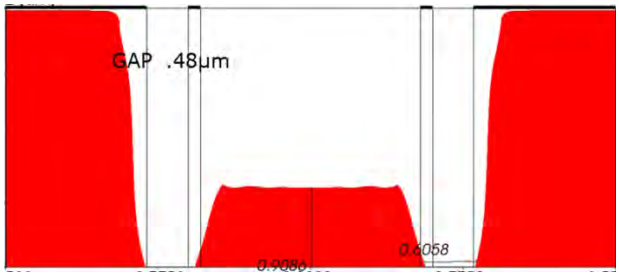



Figure 4. expected resist shape by simulation

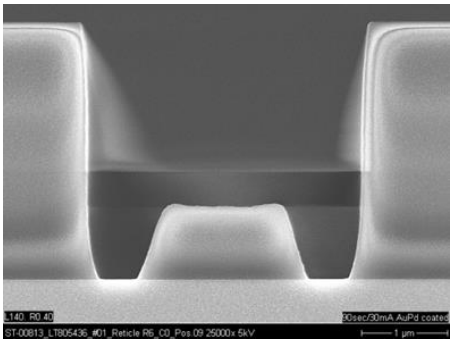


Figure 5. cross sections of resist mask

The results, obtained with the simulation based test mask, demonstrate a very good agreement of simulation with experimental data, as shown in figure 5. The variability of our grayscale process is determined to ±100nm for the resist gap between island and main structure; ±75nm for the reduced resist height with a resist taper of approximately 70°. Following this results a mask with the described grayscale process for the deep p-body implant of a 32V DMOS device is implemented in the productive workflow of one of our 130nm technologies. First inline results of this integrated hardware is expected in may 2018.

[1] Patent: DE102014100055A1; Feick, Henning; Heller, Marcel; Kaiser, Dieter; Schneider, Jens; Infineon Technologies AG

# Towards Fab Cycle Time Reduction by Machine Learning based Overlay Metrology

Faegheh Hasibi*[a], Leon van Dijk[a], Maialen Larranaga[a],
Auguste Lam[b], Anne Pastol[a], Richard van Haren[a]

[a]ASML Netherlands B.V., De Run 6501, Veldhoven 5504 DR, Netherlands
[b]STMicroelectronics Crolles, 850 rue Jean Monnet, F-38926 Crolles Cedex, France

## ABSTRACT

Overlay is one of the most critical design specifications in semiconductor device manufacturing as it directly affects yield, device performance and reliability. Monitoring and controlling the overlay performance during manufacturing is therefore of uttermost importance. Measuring the overlay performance of every exposed wafer is not possible as it implies a high cost and it may cause time delays in the fabrication process. As a result, a compromise is typically achieved by sampling the overlay metrology, for example by measuring the overlay on only a few wafers per LOT. However, for statistical process control, outlier detection, and even overlay control, it could still be very beneficial to have a good and reliable estimate of the overlay performance of the wafers that have not been measured.

In this work, we aim to develop virtual overlay metrology for the wafers that have not been measured by predicting its overlay. Building a model for overlay prediction that can be used in a high volume manufacturing environment is a highly non-trivial task as there are many sources for overlay errors. Examples of such errors are the scanner performance, the matching of scanners, the mask pattern placement errors, and other non-lithography process steps during manufacturing. Even when all the overlay contributors are known, we are left with a high dimensional feature space, which makes it difficult to build a model with high predictive power.

To make the problem tractable, we limit ourselves in this work to overlay prediction of a series of implant layers. These implant layers are exposed and processed consecutively within a few days. Every implant layer is exposed by aligning to the same bottom layer. Also overlay is measured with respect to this layer and the overlay target is at the same location for each implant layer. Furthermore, no significant impact on the wafers is expected from the ion implantation steps, e.g. wafer or mark deformation. Therefore we expect that the difference in overlay between the various implant layers is mainly determined by the scanner performance, matching of scanners and mask effects.

* Faegheh.hasibi@asml.com; phone +31 615196099

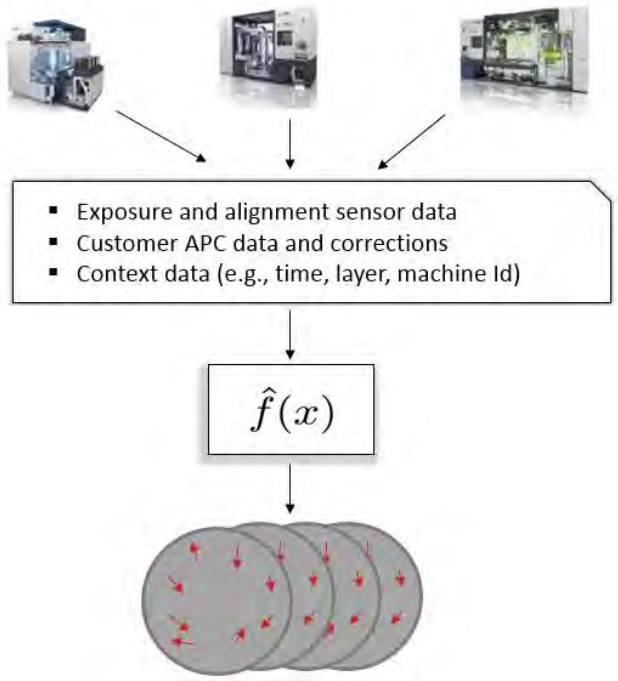



**Figure1. Example of data flow used for training the machine learning algorithm.**

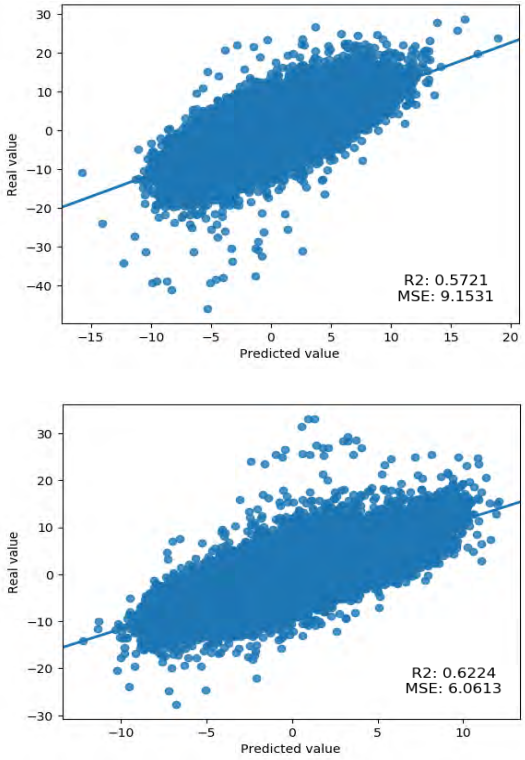



**Figure 2. Prediction performance for overlay mis-registrations in axes X (top) and Y (bottom). Each plot compares the measured and predicted values. The correlation is reported with respect to $R^2$.**

In order to build a prediction model for overlay we make use of machine learning algorithms. Machine learning, and in particular Neural Networks algorithms have changed the landscape of computational modelling over the past years. They can learn non-linear models directly from data and are shown to be effective in addressing complex problem in the neighboring areas of physics. We collect scanner, APC, and contextual data (e.g., machine and product information) from a production fab and perform through-stack prediction for nine implant layers; see Figure 1 for illustration. Our model predicts the overlay error (i.e., mis-registrations in axes X and Y) for the measured targets on the wafer. Starting from a simple linear model (using LASSO algorithm), we show prediction performance improvements using complex non-linear model using Random Forests and Neural Network algorithms. Furthermore, our models make use of the physical concepts of overlay to capture the scanner and chuck fingerprints. Figure 2 presents our preliminary results, comparing the measured and the predicted overlay with respect to the $R^2$ coefficient of correlation. We envision that accurate virtual overlay metrology improves overlay control and reduces the cycle time in the production fabs.

# Fabrication of nanoparticles for biosensing using UV-NIL and lift-off

Tina Mitteramskogler[a*], Michael Haslinger[a], Astrit Shoshi[b], Hubert Brueckl[b], Michael Muehlberger[a]
[a]PROFACTOR GmbH, Im Stadtgut A2, 4407 Steyr-Gleink, Austria
[b]Danube University Krems, Department for Integrated Sensor Systems, Viktor Kaplan Str. 2 E 2700 Wiener Neustadt, Austria

A novel technique to realize large quantities of stacked multifunctional anisotropic nanoparticles with narrow size distribution is presented. Through the combination of Ultraviolet Nano-Imprint Lithography (UV-NIL), physical vapor decomposition and subsequent lift-off processes we disperse these particles in solution to carry out biomolecular sensing[1].

Compared to other nanoparticle fabrication methods our approach holds several advantages. First, one can control the nanoparticle shape by choosing an appropriate mask for the UV-NIL process. Second, we can choose the composition of the nanoparticles as the materials are deposited layer wise by physical vapor deposition. Third, we can synthesize nanoparticles with precise geometry and very small geometrical variations. This is in contrast to chemical synthesis methods where the layer thicknesses and particle size distribution are harder to control. Due to the use of vapor deposition, a broad range of materials like noble metals (Au, Ag), oxides ($SiO_2$) and magnetic substances (Fe, Ni, Co) are available to us for the stacking of all the different layers.

The target nanoparticle shape (c.f. Figure 1) is determined through the soft PDMS stamp used in the UV-NIL process. For this work, a mask with elliptical patterns or its inverse are used for imprinting the organic UV-curable prototype NIL resist mr-NIL212FC_XP[2] on top of the lift-off layer LOR1A. Both resins are spin coated on top of a silicon wafer sputtered with an aluminum-doped zinc oxide (AZO) layer. After the UV-NIL step, a break through etch to the LOR1A layer is performed in oxygen plasma followed by wet chemical etching of LOR1A in diluted MF24A in order to reach the AZO layer. This creates undercut structures on which the material deposition is performed. These undercuts aid the removal of the mask through immersion in a diluted MF24A solution, thus leaving only the nanoparticles behind as shown in Figure 3. By etching the AZO layer through a longer exposure to MF24A the particles are brought into solution and are ready for further processing. Figure 3d shows the finished nanoparticles.

The underlying homogeneous biosensing method is based on the optical detection of changes in the rotational dynamics of anisotropic hybrid nanoparticles immersed in the analyte such as whole-blood[3]. First tests reveal lowest detectable particle concentration in the picomolar (ng/mL) regime.

**Acknowledgments**

We gratefully acknowledge funding by the Lower Austria Forschungs- und Bildungsges.m.b.H. (NFB) within the Life Science Call and partly from the Federal Ministry of Transport, Innovation and Technology (BMVIT) supported by the Austrian Research and Promotion Agency (project LAMPION, #861414) and by the European Regional Development Fund in cooperation with the State of Upper Austria within the program “Investment in growth and employment”.


Figure 1. Left: Target nanoparticle layout for biomolecular sensing. Right: AFM image of the mr-NIL212FC_XP (inverse) mask with undercuts as shown in step 4) of Figure 3. The right particle is standing upright, whereas the left particle has fallen over, showing its pronounced undercut in the LOR1A.

* tina.mitteramskogler@profactor.at

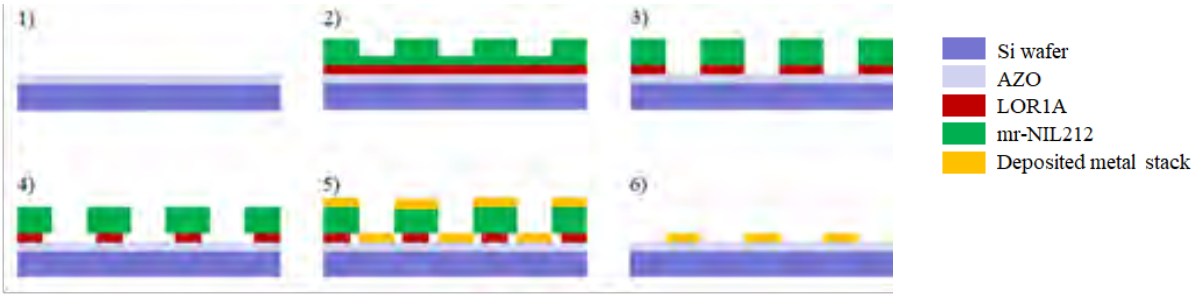
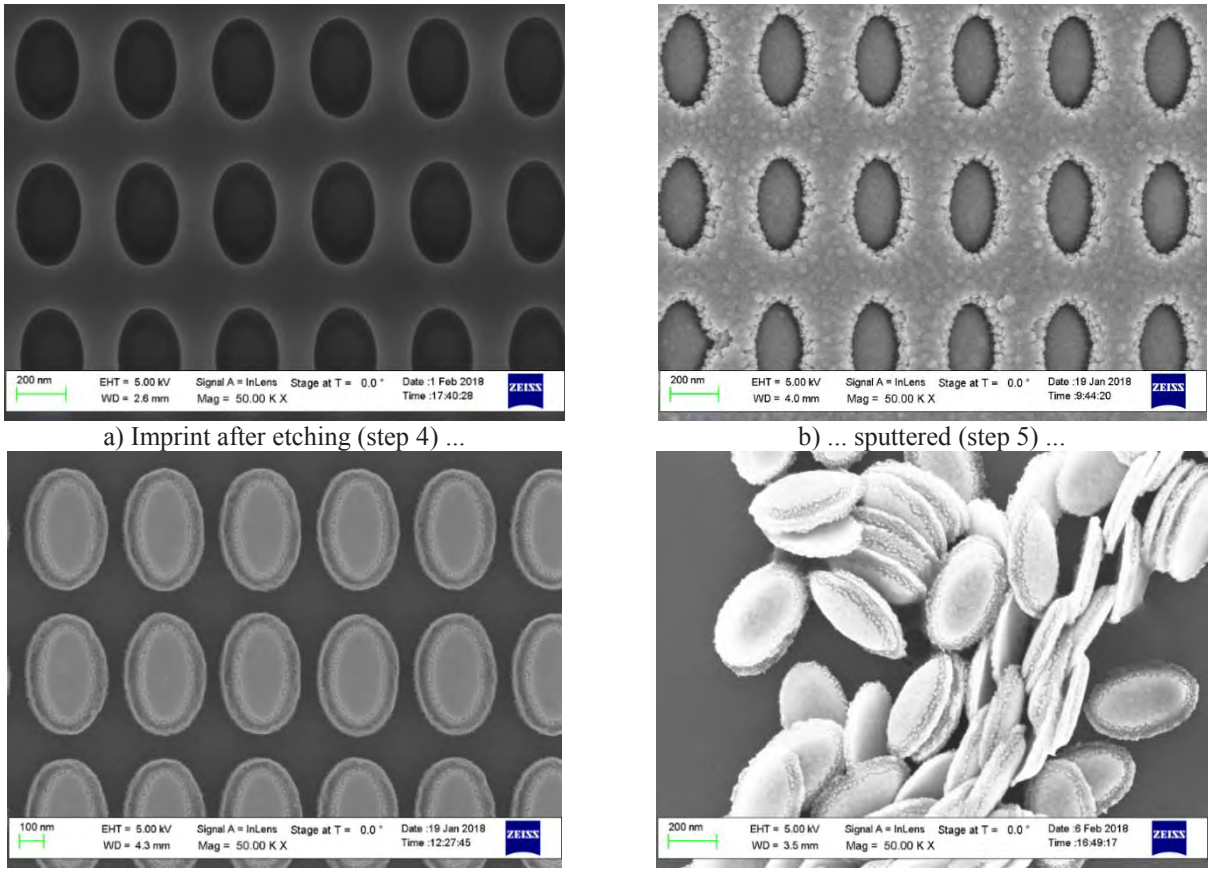



Figure 2. Schematics of our novel fabrication process. A wafer sputtered with an AZO layer (1) is spincoated with LOR1A and imprinted using mr-NIL212FC_XP with a soft PDMS stamp (2). After oxygen plasma etching (3) and wet chemical etching (4), the desired metal stack is deposited (5). Through immersion in MF24A the mask can be removed and the nanoparticles are ready for lift-off from the AZO layer (6).




a) Imprint after etching (step 4) ... b) ... sputtered (step 5) ...

c) ... mask lift-off (step 6) ... d) ... and final nanoparticles.

Figure 3. SEM images showing the process steps depicted in Figure 2.

[1] Shoshi, A., Schneeweiss, P., Haslinger, M. J., Glatzl, T., Kovács, G., Schinerl, J., Muehlberger, M. and Brueckl, H., "Biomolecular Detection Based on the Rotational Dynamics of Magneto-Plasmonic Nanoparticles," Proceedings **1**(4), 541 (2017).

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# Dry etching challenges for high-χ block copolymers

P. Bézard[a], X. Chevalier[b], C. Navarro[b], C. Nicolet[b], G. Fleury[c], I. Cayrefourcq[b], R. Tiron[d], M. Zelsmann[a]

[a] Univ. Grenoble Alpes, CNRS, LTM, Mintaec campus, 17 rue des martyrs, 38000 Grenoble, France
[b] ARKEMA, Groupement de recherches de Lacq, 64170 Lacq, France
[c] LCPO, CNRS–ENSCPB–Université de Bordeaux, 33607 Pessac, France
[d] CEA-LETI, Mintaec campus, 17 rue des martyrs, 38000 Grenoble, France
e-mail: marc.zelsmann@cea.fr

*Summary:*
*In this work, we present our recent achievements on the integration and transfer etching of a novel silicon-containing high-χ block copolymer for lines/spaces applications. Developed carbo-silane BCPs are synthesized under industrial conditions and present periodicities as low as 14 nm. Thanks to the development of dedicated neutral layers and top-coats allowing perpendicular orientations, it was possible to investigate specific plasma etching processes on full-sheets at 7 nm resolution, opening the way to the integration of these polymers in chemo-epitaxy stacks.*

Block copolymer (BCP) with highly incompatible segments (so-called high-χ BCPs) are attractive as a complementary next generation lithography technique since they can create self-assembled periodic patterns with features sizes below 10 nm. However, this high incompatibility is not without drawbacks, including for example long thermal annealing or preferential wetting at interfaces of one of the blocks. Then, forming perpendicular lamellar morphologies, which is the most promising approach for nanopatterning in terms of critical dimension control and resist budget, becomes a difficult task. At the substrate's interface, such an orientation is usually obtained with a grafted random copolymer with the same chemistry as the BCP but at the top interface complicated top-coat approaches have to be pursue since the solvent used for the top-coat should not remove the BCP layer. These development are of particular interest for the so-called "chemo-epitaxy" directed self-assembly (DSA) approach, were high resolution chemical pre-patterns are used to ensure large scale registration of the formed micro-domains.
In the present study, we report on the use of a new type of high-χ BCP: Poly(styrene)-block-Poly(1,1-dimethyl silacyclobutane) (PS-b-PDMSB, Fig. 1). This polymer showed lamellar periodicities down to at least 14 nm and its Flory-Huggins parameter χ was evaluated in the range 0.08-0.1 at room temperature. A low glass transition temperature silicon-containing block is chosen here in order to improve the self-assembly kinetics. Also, this block copolymer can be synthesized in industrial conditions with an extremely low metal contamination and a high etch resistance of the Si-block is anticipated without additional processing steps (infiltration).
However, the integration of a BCP into a chemo-epitaxy process-flow does require neutral materials for the top and bottom interfaces of the film in order to provide perpendicular BCP's features. In this view, Arkema developed various materials to satisfy neutrality conditions and other requirements inherent to microelectronic processes (Fig. 1). For instance, the underlayer and the top-coat materials are both silicon-free so as to maximize and optimize the available aspect-ratio of perpendicular silicon-containing features versus etch-plasma chemistry for transfer into the underlaying substrate. These materials are also designed so as to be processed under standard time and temperature conditions of regular microelectronic processes to ensure a high throughput of silicon wafers (i.e. the neutral underlayer can be grafted following a process at 200°C during 75 seconds). An example of cross-section STEM imaging of a 7 nm half-pitch polymer (thermally annealed at 160 °C for 5 min to initiate the self-assembly) sandwiched between a grafted neutral underlayer (4 nm thick) and a 20 nm thick top-coat is given in Fig. 2.
Top-coat, PS and neutral underlayer are removed by dry-etching in a 300 mm industrial plasma reactor (Applied Materials). A pure $Cl_2$ plasma chemistry is used for top-coat and BCP layer etching, providing a good control on both selectivity and etch rate. The etch rate of the BCP film can be independently adjusted from the selectivity between blocks. Examples of BCP surfaces at this step for two polymers are reported in Fig. 3. Then, an additional $Ar/O_2$ step is performed to remove the PS block and oxidize the PDMSB block. By using Argon-rich gas mixtures, one can sufficiently modify the PDMSB block and no collapse of the lines is observed as illustrated in Fig. 4 (left). In order to limit the impact on well-known microloading effects, a $Ar/HBr/N_2$ plasma chemistry is preferred to $Ar/O_2$ to etch the grafted neutral underlayer. Though promising, early tests of silicon transfer with a standard process show greater roughness than after BCP reveal (Fig. 4 right). This roughness is due to the redepositing of etch products and optimizations are undergoing in other plasma chemistries designed for non-sticking etch products.
**Acknowledgements:** The research leading to these results was partly supported by the French RENATECH network, by the French LabEx Minos ANR-10-LABX-55−01, by the European ENIAC JU project PLACYD and by the French FUI project REX-7.
**Keywords:** Directed Self-Assembly, PS-*b*-PDMSB, neutral layers, plasma etching

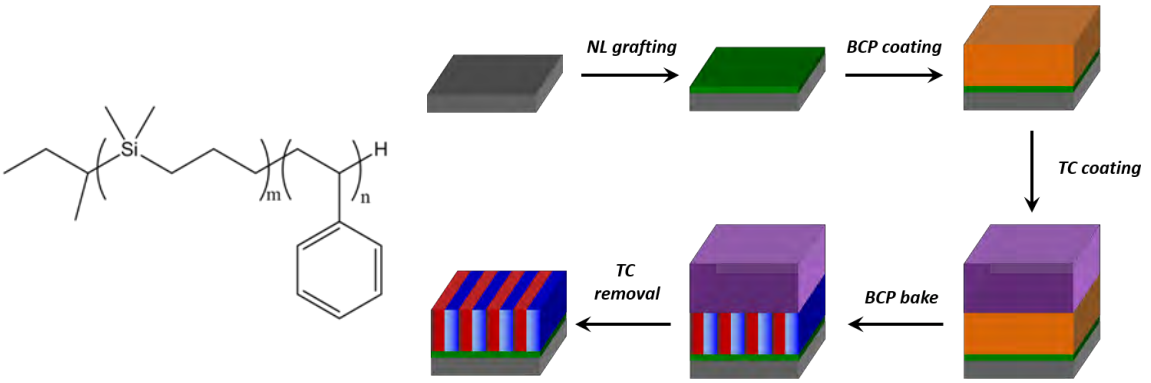


Fig. 1. Chemical formulae of used lamellar PS-b-PDMSB and schematic of the process used to obtain perpendicular lamellas using a grafted neutral layer (NL) and a neutral top-coat (TC)

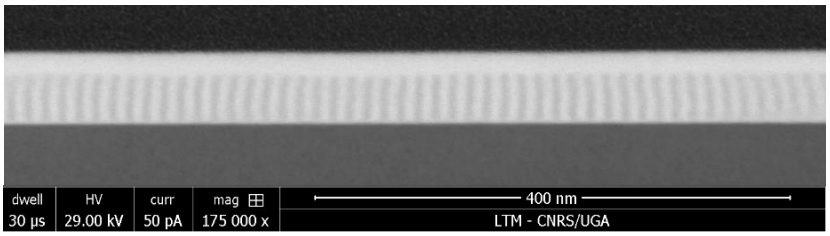


Fig. 2. Cross-section STEM image of a 14 nm period, 40 nm thick PS-b-PDMSB layer thermally assembled between a neutral underlayer and a neutral top-coat onto a silicon wafer

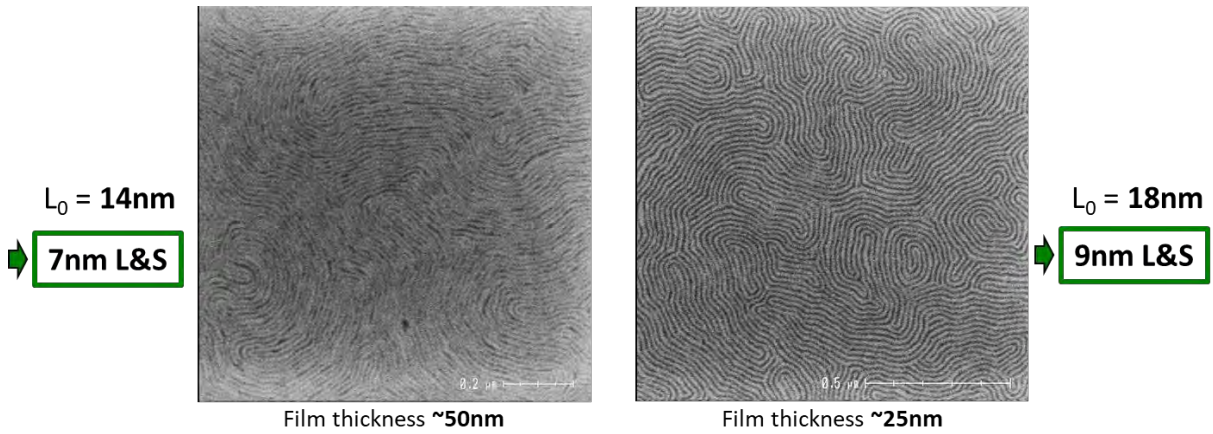


Fig. 3. Top-view SEM observations of two different polymers (14 and 18 nm periods) after removing the top-coat and a 5s-long Ar/O2 plasma for PDMSB revelation

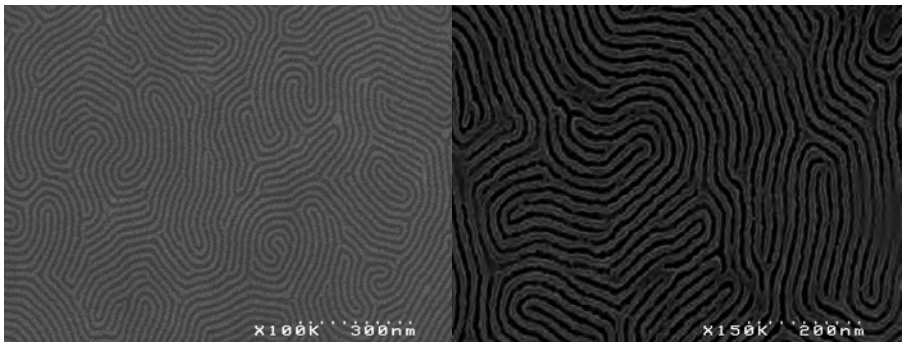


Fig. 4. Top-view SEM images of the 18 nm period polymer after removing the top-coat in a $Cl_2$ plasma chemistry and etching the PS block in a $Ar/O_2$ chemistry (left), and after first attempts at transferring theses PDMSB features into the silicon wafer (right)

EML18-EML100-4.

# Machine learning methods applied to process qualification

**Authors:**
**Mark Herrmann**
**Stefan Meuseman**
**Clemens Utzny**
**Advanced Mask Technology Center GmbH & Co. KG**
**Rähnitzer Allee 9 D-01109 Dresden**
**Germany**

Corresponding author: Clemens Utzny

**Abstract:**
With the substantial surge in the need for high end masks it becomes increasingly important to raise the capacity of the corresponding production lines. To this end the efficient qualification of matching tools and processes within a production line is of utmost relevance.

Matching is typically judged by the processing of dedicated lots on the new tool and process. The amount of qualification lots should on the one hand be very small, as the production of qualification plates is expensive and uses capacity of the production corridor. On the other hand the strict requirements of high end products induce very tight specification limits on the matching criteria. It is thus often very difficult to assess tool or process matching on the basis of a small amount of lots.

In this paper we expound on a machine learning based strategy which assesses the mask characteristics of a qualification plate by learning the typical behavior of these characteristics within the production line variations. We show that by careful selection of reference production plates as well as by setting specification limits based on the production behavior we use a small amount mask in order to manage the qualification tasks efficiently.

The specification characteristics as well as the specific limits are selected and determined using a naïve Bayes learner. The resulting performance for prediction of tool and process matching is assessed by considering the resulting receiving operator curve. As a result we obtain an approach towards the assessment of qualification data which enables engineers to assess the tool and process matching using a small amount of matching data under the constraint of substantial measurement uncertainties.

As an outlook we discuss how this approach can be used to examine the reverse question of detecting process failures, i.e. the automated ability to raise a flag when the current production characteristics start to deviate from their typical characteristics.

Overall, in this paper we show how the rapidly evolving field of machine learning increasingly impacts the semiconductor production process.

## Using a naive Bayse for the qualification of back up tools and processes

The similarity of spatial signatures can be assessed by various measures, such as the range of the difference between tow signatures or their shape similarity as measured by a suitably constructed AUC. Each of these measures has its specific properties. A measure which fails to detect significant differences for one type of deviation, may be powerful in discriminating a between two distinct signature where all other measures fail.
In this paper it is explained how the systematic study of various measures leads to a final set of three measures with distinct properties in measuring the similarities and differences between process signatures.
In order to derive a threshold value for the distinction of matching and non-matching tools a Bayes classifier is training using the final set of covariates. Threshold values are derived with the resulting probabilities for matching/non-matching (see Figure 1)).

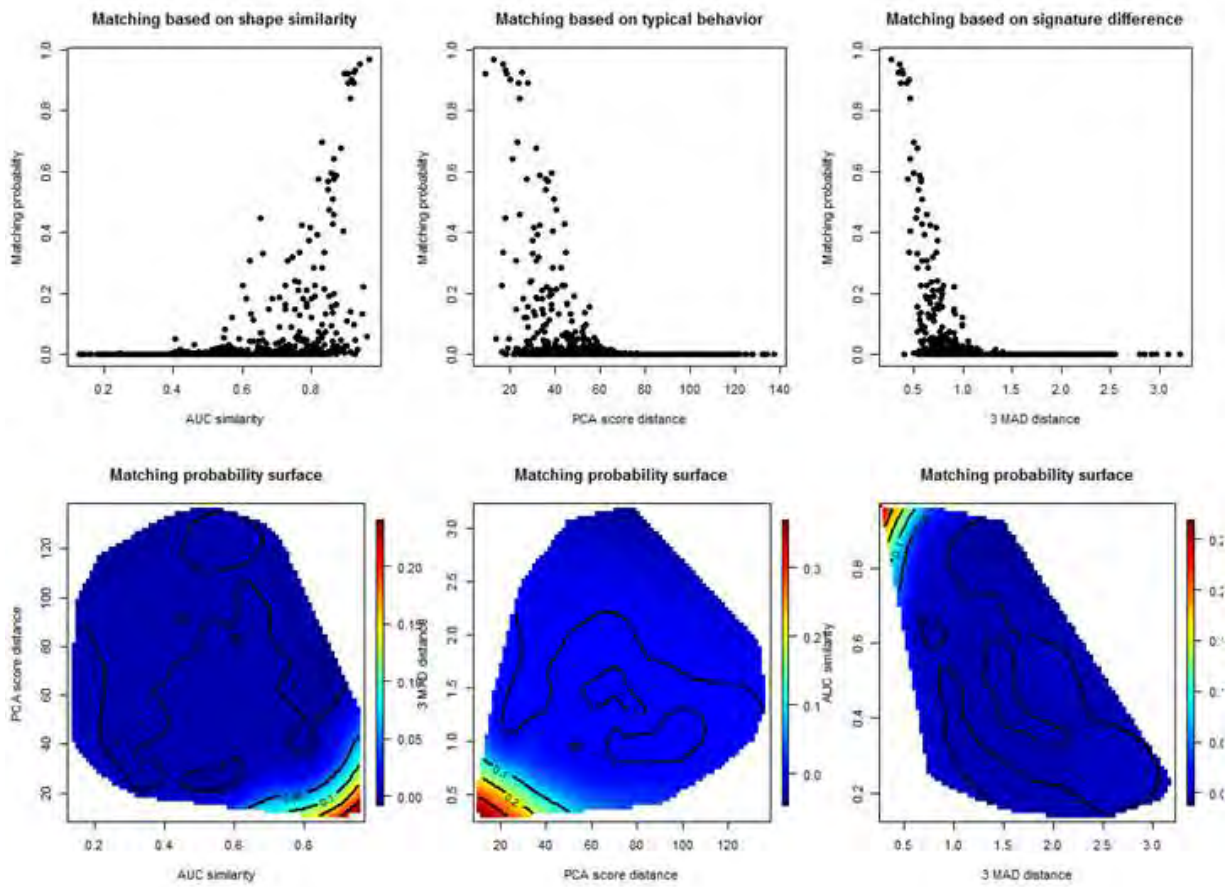


*Figure 1) The matching probabilities as computed by the naive Bayes classifier are depicted. The upper panels show the matching probabilities over the AUC shape similarity measure (left), the PCA assessment of the typical behavior (middle) and the MAD measure of the signature difference. The lower three panels give the probability surfaces as cuts through the plane. It is clearly demonstrated that the probability of matching increases when the AUC is above 0.8, the PCA distance is below 45 and the 3 MAD distance is below 1.25nm.*

# Deposition Durability of e-Beam Mask Repair

**Christian Holfeld[2] ; Tim Göhler[1] Pavel Nesladek[1] Thorsten Krome[1]**

1) **Advanced Mask Technology Center GmbH & Co. KG, Rähnitzer Allee 9 D-01109 Dresden, Germany**

2) **GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, Wilschdorfer Landstr. 101, 01109 Dresden, Germany**

Even though strong efforts are undertaken to reduce the defect count on high-end masks, the number is often not zero. Since those defects might print on the wafer and hence affect the purpose of the product negatively, the repair is frequently needed. Depending on the nature of the pattern deviation from its intended shape one typically distinguish between opaque and clear defects. Where on the one hand opaque defects are removed by either mechanical work of an AFM, laser-repair or beam-assisted local etch the repair of clear defects on the other hand is generally carried out by depositing a precursor using an e-beam repair or a focused ion beam tool.

Ideally this deposition (short "*depo")* resembles the absorber material in chemical and physical properties especially in the optical ones. However to match the optical properties certain trade-offs have to be made because in general the deposited material is not the same as the absorber. As a consequence for example the height of the deposition stack might differ from the actual absorber height. Whereas such differences can be compensated e.g. by applying a bias to the repair shape and checked by qualification methods like AIMS there is another aspect which could evolve critically during mask usage: the durability of the deposition.

Common mask cleaning processes for instance can impair or even remove the deposition depending on the process parameters. Potentially even more critical is the change of depo repairs during DUV exposure. Such evidence together with the mechanism behind has already been reported over a decade ago. Despite all the progress of the repair processes which have been made this issue is still valid nowadays in particular for high volume manufacturing (HVM) where the masks typically gather significant dose during lifetime.

In this work we monitored the change of transmission and CD of various repaired clear defects during the mask usage in the wafer fab. To obtain those numbers we frequently revisited the repair spots using an AIMS tool in the mask shop and recorded the change of transmission and CD over the dose the masks has accumulated in the meantime. We observed a more or less strong degradation depending on the following factors: the size and location of the defect within the pattern, the repair-tool used and the applied dose at the scanner. To rule-out the effects of location and size of the defect we compared the depo processes of two different e-beam repair tools at the same defect after replacing the depositions with the other tool. The change has been normalized considering the different dose. Thus we assessed the durability of the depositions placed with the different processes/tools.

The results show, how important it is to closely monitor the depo repair spots over the lifetime of the mask particularly if it comes to HVM. The inline inspection of the mask in between wafer starts might give a first hint if a deposition is degrading, the actual extend of

the change and the printing behavior can be quantified using the AIMS. We also show, that failing depo repairs can be reworked and often sealed with a more durable deposition.

As an outlook one could adopt the more reliable deposition strategy also for older repair tools in the field – even if the chemistry is not completely identical. Moreover the topic gives rise to the question on how depositions during EUV exposure are behaving, which could be the subject of further investigations.

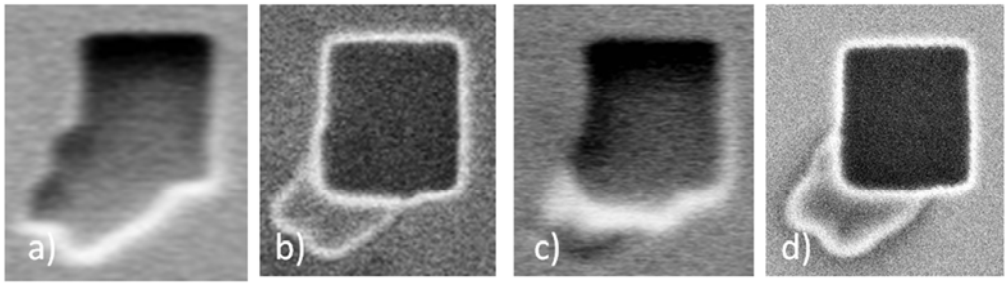


*Figure 1: a) clear defect before repair, b) defect right after repair using tool A, c) deposition after DUV exposure, d) new deposition using tool B*

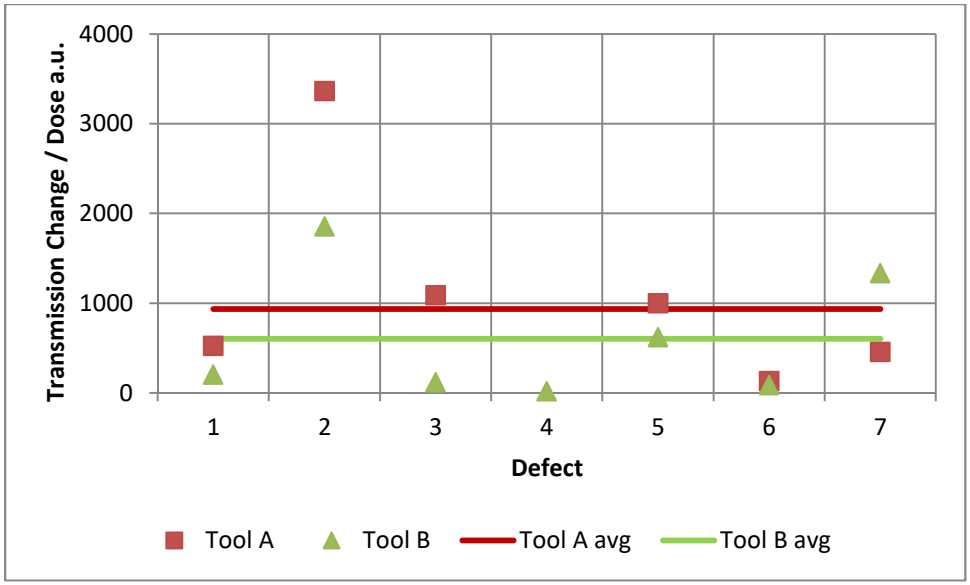


*Figure 2: This plot shows the change of transmission per applied dose for 7 defects which have been repaired by a deposition placed with two different e-beam repair tools and processes (Tool A and B). Except for one repair (Def#7) the deposition of tool B are obviously less prone to degradation than those of tool A.*

# Nikon's Large-Size Photomask Blanks for Production of High Resolution Panels

Takashi Yagami, Yohei Takarada, Kento Hayashi and Takashi Ozawa
Nikon Corporation
10-1, Asamizodai 1-chome, Minami-ku, Sagamihara-city, Kanagawa 252-0328, Japan
Phone: +81(42)-740-6471, e-mail: Takashi.Yagami@nikon.com

## ABSTRACT

Nikon has manufactured silica glass ingots, substrates and blanks for FPD photomask. The liquid crystal display (LCD) and organic light emitting diode (OLED) panels are progressing every year with larger size and higher resolution. Along with that, large size and high accuracy are required for FPD photomask.

Nikon has excellent surface control technology of FPD photomask substrates over G10 area, as a result of Nikon's polishing technology and deflection simulation. In this study we introduce our "Super Flat Mask (SFM) series" and "Bending Mask". Fig. 1 shows the excellent flatness of Nikon's SFM-SS over G10 area. Bending Mask has the special shape which can cancel the deflection under its own weight.

High accuracy measurement machine is required for guarantee of higher flatness. We have developed our own flatness measurement machine, "ALGS". ALGS can measure the flatness more accurately than the conventional machine (Fig. 2).

Additionally we also introduce our Cr Binary and Att-Phase Shift film over G10 area. These films have uniform optical characteristics and nearly orthogonal cross section after etching. Not only substrates with excellent flatness, these films also enable to produce high resolution panels.

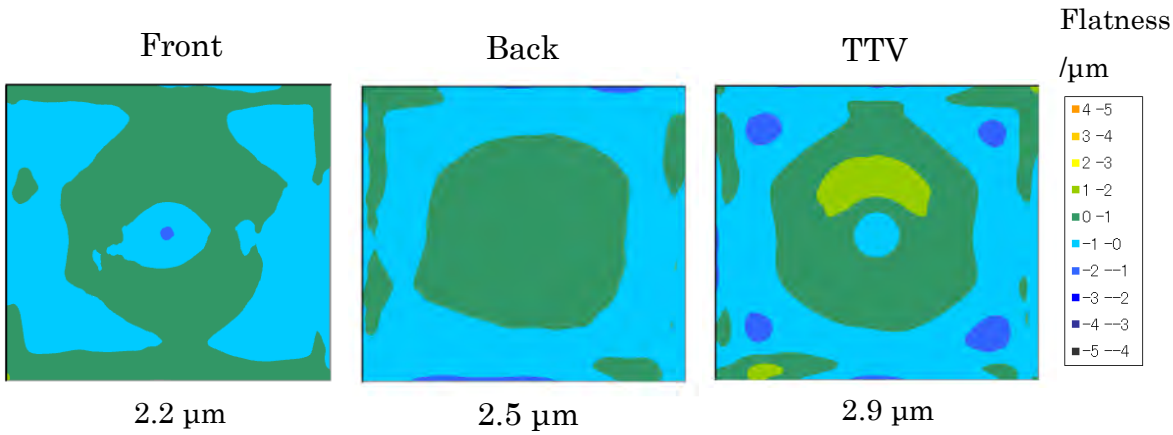


Fig. 1 Flatness of Nikon's SFM-SS over G10 area

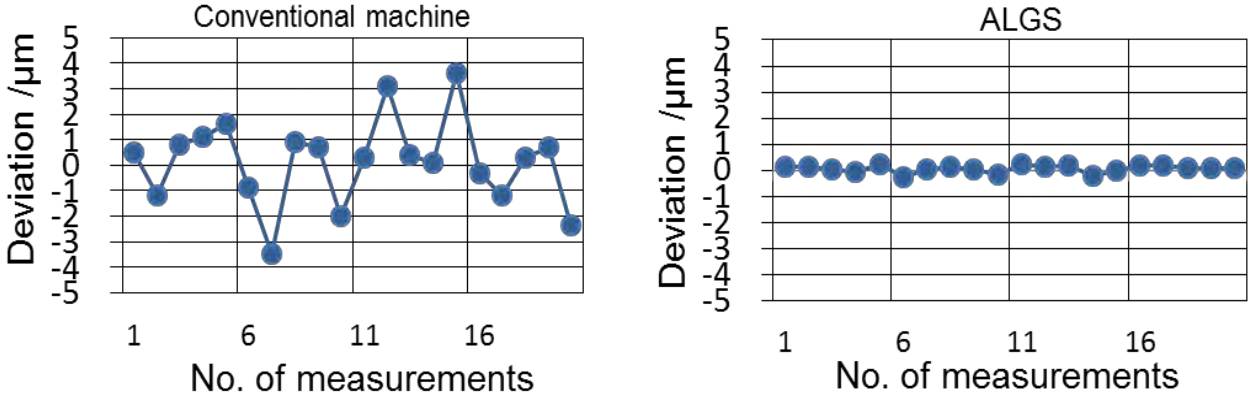


Fig. 2 Measurement accuracy of ALGS

# Maximizing Utilization of Large-Scale Mask Data Preparation Clusters

Pascal Gilgenkrantz[a], Stephen Kim[b], Wooil Han[c], Minyoung Park[b] and Min Tsao[b]
[a] Mentor Graphics (Ireland) Ltd. French Branch 110 rue Blaise Pascal, 38334 St Ismier, France
[b] Mentor Graphics Corp. 46871 Bayside Parkway, Fremont, CA 94538, USA
[c] Mentor Graphics (Korea) LLC. 7F Pangyo Mirae Asset Center 12,
Pangyoyeok-ro 192beon-gil, Bundang-gu, Seongnam-si, Gyeonggi-do, 13524 Korea

## ABSTRACT

With CMOS technology nodes going further into the realm of sub-wavelength lithography, the need for compute power also increases to meet runtime requirements for reticle enhancement techniques and results validation. Expanding the mask data preparation (MDP) cluster size is an obvious solution to increase compute power, but this can lead to unforeseen events such as network bottlenecks which must be taken into account. Advanced scalable solutions provided by optical proximity correction (OPC)/mask process correction (MPC) software are obviously critical, but other optimizations such as dynamic CPU allocations (DCA) based on real CPU needs, high-level jobs management, real-time resource monitoring, and detection of bottlenecks are also important factors for improving cluster utilization in order to meet runtime requirements and handle post tape-out (PTO) workloads efficiently. In this paper, we will discuss tackling such efforts through various levels of the "cluster utilization stack" from low CPU levels to business levels to head towards maximizing cluster utilization and maintaining lean computing.

**Keywords:** MDP, OPC, DCA, PTO, compute cluster, runtime, optimization

## INTRODUCTION

PTO flow is composed of the steps required to transform an integrated circuit (IC) tape-out to data format suitable for photolithography masks manufacturing, and ensures that these steps will translate into good yield in fab through a large process window. Steps include layer extraction, retargeting, OPC, MPC, fracture, and rules- or model-based verification. Each new CMOS technology node requires more complex operations especially for OPC and MPC. These operations use computational lithography[1] emphasizing the growing importance of computation for photolithography in microelectronics manufacturing and complementary to the advances in materials and systems. Computational lithography has high CPU power needs leading to usage of high-performance computing clusters of growing size in the range of tens of thousands of CPU cores towards hundreds of thousands of CPU cores. This creates the potential for bottlenecks at every level from individual CPU to operating system, network, and cluster. However, growing CPU power needs are not the only trend: more and more intelligence is also required to increase the "useful" CPU power proportion as flat-mode lithographic simulations are too compute-intensive to be used for all critical masks. Multiple approaches making the best possible use of initial design hierarchy have been introduced [2, *other references needed*] with the drawback that each individual operation has its own scalability potential. This individual scalability potential needs to be taken into account by distributing CPU power dynamically between jobs in order to increase the cluster utilization. This is a global task that can be addressed only from an upper-level perspective in the job scheduler level and the cluster monitoring tools. The flexibility required in a production environment as well as the job robustness must also be considered in order to maximize the utilization of such large-scale MDP clusters.

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# Best Practices Leveling, Vibration and for Reducing Reticle Haze in 193nm Reticle Scanner Environments

Allyn Jackson

CyberOptics Semiconductor Division, Minneapolis, MN, USA
ajackson@cyberoptics.com

The importance of reticle leveling, vibration and relative humidity control has rarely been considered in reticle environment. However, the need to maximize both yields and tool uptimes in reticle mask environments requires best-in-class practices.

Whether for diagnostics, qualification or preventative maintenance, equipment engineers need to efficiently and effectively make measurements and adjustments to the tools. In reticle environments the vibration, leveling and RH measurement methods are typically cumbersome, non-representative, not real time, compromise the production environment and are costly with downtime required to take the tool offline for these tasks. By contrast, best practice methods involve collecting and displaying acceleration, vibration and humidity data in real-time, speeding equipment alignment or set-up. Real-time data also speeds equipment diagnostic processes saving valuable time and resources. Equipment engineers can also make the right adjustment time after time with objective and reproducible data that essentially enhances process uniformity.

**Reticle Haze - Background:**
ALL 193nm scanners are adversely affected by "Haze" when proper measures are not taken to control it. AMSR can be used as a critical tool in measuring and controlling H2O which in turn reduces Haze and increases Reticle lifetime.

**"Haze", H2O and 193nm Scanner Environments** (i.e. all Immersion Scanner Environments)
When not controlled in 193nm scanner environments, Haze forms on reticles and shortens the reticle lifetime. All 193nm scanners are affected by this phenomenon called Haze and identifying sources of H20 in these scanners is critical to helping prevent Reticle Haze.

**Summary:**
There are three areas that need to be controlled to reduce and/or control Haze on Reticles:

1. Mask residue / Acid (controlled by cleaning procedures, etc…)
2. 193nm light (can't be controlled because needed)
3. Water/Humidity (this is where a reticle-like RH sensor is needed))

To control H2O in 193nm scanners they are purged with XCDR – Extra-clean Dry Air or N2. The below pic and in the attached shows the formation of Haze with H2O at 10,000ppm and less than 1000ppm. The solution here is that a reticle-like wireless reticle-like RH, vibration and leveling sensor can be used to verify Dry environments in any reticle area the reticle travels and consequently be exposed to H2O.

Potential Areas that Reticles could be exposed to H2O are not just inside the Scanner and include:

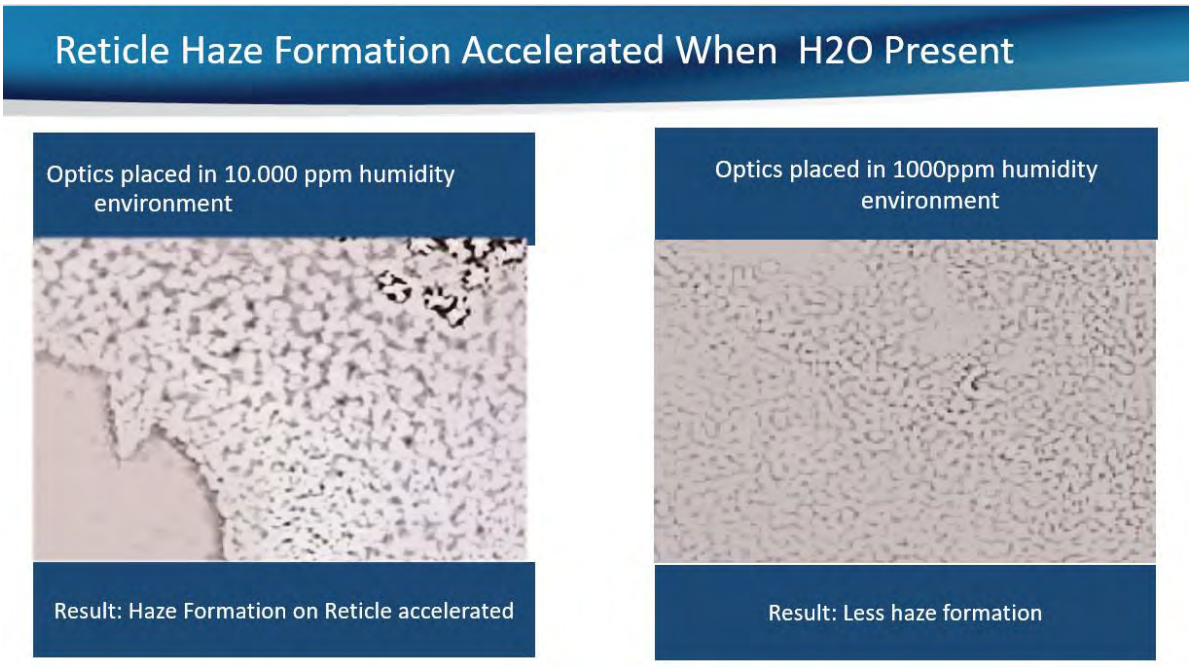
1. Reticle Library
2. Reticle Stage

3. Reticle Stocker
4. Reticle Handling in general
5. RSPs (regularly cleaned with water and need to be verified dry before returning to production)
6. Any place the Reticle goes where water could attached itself to the reticle

The current method for checking RH in the above locations are in-situ Rh sensors (in some places) and
hand-held RH sensors. The problems with the current methods of measuring for RH include:

1. In-situ RH sensors are not everywhere and the problem with hand-held RH sensors are the following:
2. Hand-held RH sensors are Inconvenient
3. Hand-held RH sensors compromise the reticle environment
    a. For example, if Scanner panels are opened, if might take hours to requalify the tool before going back on line
    b. Opening chambers, stockers, RSPs, etc.. where Reticles travel contaminates the environment being tested
4. Many reticle areas that should be checked for RH are inaccessible by hand-held RH sensors and in-situ Rh sensors are impractical

The ReticleSense AMSRQ wireless humidity, leveling and vibration measurement reticle; allows for measurements under actual Reticle environment conditions.




This poster and discussion will review the advantages of using a wireless, real-time, reticle-like device for key measurement applications in reticle mask environments that delivers on three compelling bottom lines – saving time, saving expense and improving yields.

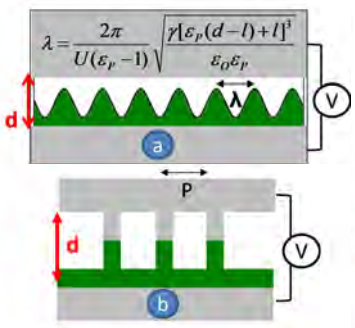
# ElectroHydroDynamic Lithography for complex polymer structures

**C. Gourgon, J.H. Tortai, J. Boussey, M. Panabière, S. Labau**

**Laboratoire des Technologies de la Microélectronique – CNRS-UGA-Minatec**
**17 R. des Martyrs, 38 054 Grenoble Cedex - France**

Polymer micro and nanostructuration is commonly achieved using standard lithography techniques such as optical lithography, E-beam lithography or NanoImprint Lihtography (NIL). These techniques are nevertheless not adapted to the fabrication of complex shape patterns or polymer structuration on non-flat surfaces. One example is the realization of microlenses for sensors applications. ElectroHydroDynamic Lithography (EHDL) is an alternative to this limitation. A low viscosity or molten polymer surface deforms spontaneously when it is submitted to an electric field, resulting in periodic patterns whose period depends on polymer properties such as its dielectric permittivity and surface energy, polymer thickness, the air gap between the polymer surface and the upper electrode, and of course on the electric field amplitude. This principle is illustrated on figure 1a. The deformation is enhanced by polymer heating to decrease its viscosity, or by the use of low viscosity monomers that can be UV crosslinked after spontaneous structuration. If the top electrode is patterned as illustrated on figure 1b, the polymer deforms to duplicate the electrode structures and the patterns profiles can be controlled by some parameter optimization. Several publications present simulation results on this technique [1-2], and few papers demonstrate the use of EHDL to fabricate polymer structures for various applications such as bifocal lenses [3].

In this paper we demonstrate experimentally the influence of polymer thickness on pattern structuration, as illustrated on figure 2. A positive duplication is obtained when the spontaneous period $\bar{}$ is inferior to the period of the template patterns, whereas a filling of template cavities occurs in the opposite case. We will show that this behavior is in good agreement with simulation. We will also present the influence of nanoparticules embedded in the polymer and the impact of electrode material. The scenario of pattern formation will be explicated and perspectives of EHD lithography will be reviewed.



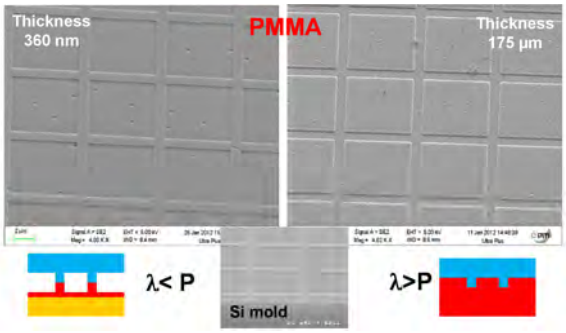




Figure 1: principle of EHDL Figure 2: influence of polymer thickness

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# Plasmonic Resonances in Metal Covered 2D Hexagonal Gratings Fabricated by Interference Lithography

Andrei A. USHKOV[1, a)], Maxime BICHOTTE[1], Isabelle VERRIER[1], Thomas KAMPFE[1], Yves JOURLIN[1]

[1]*Univ Lyon, UJM-Saint-Etienne, CNRS, Institut d'Optique Graduate School, Laboratoire Hubert Curien UMR 5516, 42023, Saint-Etienne, France*

[a)]Corresponding author: andrei.ushkov@univ-st-etienne.fr

**Abstract.** We present both modeling and experimental results devoted to design, fabrication and characterization of metal covered hexagonal diffraction gratings. Variation of exposition and development time allow to modify the shape of the elementary cell, leaving the depth and periodicity unchanged. Fabrication process was modeled using real parameters of lithography bench and the photoresist, what substantially improved experimental results. The high quality of metal covered gratings is confirmed by excitation of plasmonic resonances, which are in a good agreement with theoretical predictions. Described approach allows to better understand plasmonic effects in 2D periodic structures and lead to an optimized design of plasmonic sensors.

## 1. INTRODUCTION

A big variety of fabrication technologies have been developed for the needs of nanostructure research: different self-assembly approaches [1-2], colloidal lithography [3], laser interference lithography [4] or direct writing [5]. Laser interference lithography has a number of advantages over other techniques. As a one-shot technology in comparison with serial write approaches (e-beam, laser writer) it is typically much quicker and less expensive, it also allows to fabricate big (~$cm^2$) long-range ordered 1D, 2D structures [6] and quasicrystals [7]. For particular applications in photodetectors and photovoltaics specific resonances in 2D metallic gratings like plasmon polaritons and cavity modes [8] attract considerable attention. In this context interference lithography is a flexible tool for designing the elementary cell as it can cover a wide range of fill factors for the same resist layer. In the current work we demonstrate it with 2D diffraction gratings of different topography, from disconnected pillars to nanoholes, modeled, fabricated and measured by AFM. After metal deposition, a good correspondence was found between simulated and experimentally observed plasmonic resonances.

## 2. EXPERIMENTAL DETAILS

The experimental bench for laser interference lithography is sketched in Fig.1:

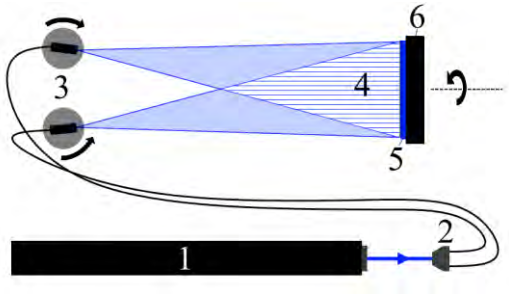
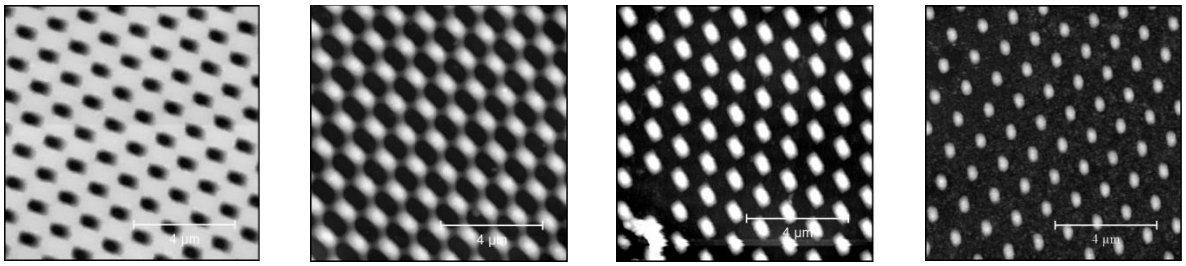



Fig.1. Scheme of interference lithography equipment: 1 – He-Cd Laser 442 nm; 2 – beamsplitter and optical fibers; 3 – step motors for beams angle control; 4 – region of two-beams interference; 5 – sample with a layer of photoresist; 6 – rotatable substrate.

Single exposition (with two interfering beams of wavelength $\lambda$, angle $\theta$ between them and the same polarizations) leads to 1D structuration of the photoresist with a period of $\Delta = \lambda / 2\sin(\theta/2)$. Rotating the substrate allows to perform multiple expositions with different angles $\alpha$ between the sample and the fringes, producing a 2D structuration.

We consider the two-exposition case with $\alpha = 60°$. This procedure leads to a 2D grating with two equal periods $\Lambda_1 = \Lambda_2 = \Delta / \sin(\alpha)$ with angle $\angle(\Lambda_1, \Lambda_2) = \alpha = 60°$ between them, i.e. an ideal hexagonal arrangement. For photosensitive layer we used photoresist S1805 of thickness ~170 nm, deposited by spin-coating on a glass substrate and pre-baked at 60 °C for 1 min before exposition. Exposition and development time varied from sample to sample in order to obtain different filling factors. Figure 2 demonstrates 4 different topographies, from pillars to holes, of hexagonal gratings with equal periods, measured by AFM:



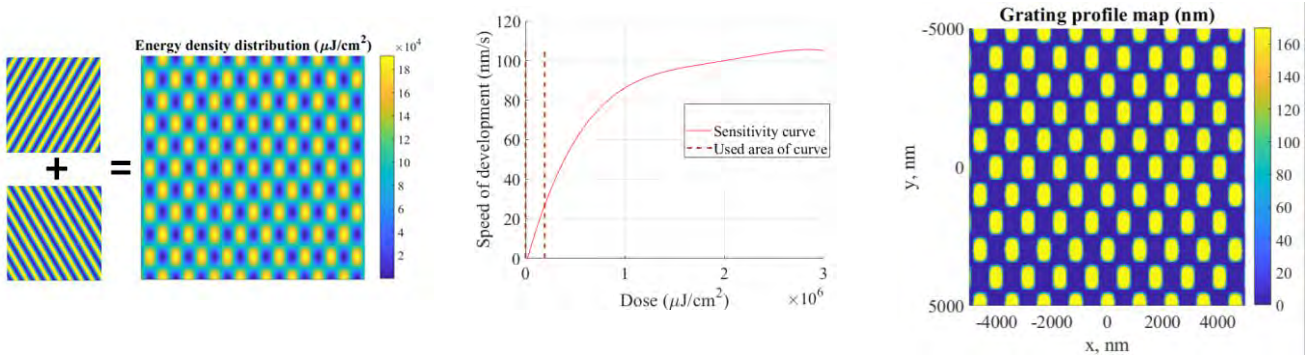

(a) (b) (c) (d)

Fig.2. AFM images of hexagonal gratings with identical periods, but different topographies, from disconnected holes at (a) to disconnected pillars at (d), fabricated by two-exposition interference lithography technique. Exposition time is increasing while moving from (a) to (d).

The metal layer (Al) was deposited by an evaporation process. The thickness of Al (~60 nm) is enough to prevent resonant transmission [9].

## 3. MODELING OF GRATING PROFILE

To predict the future shape of the elementary cell after a particular exposition and development time we calculate numerically the energy distribution map on the sample surface and employ sensitivity curves of the photoresist S1805. An example of such calculation for grating from fig.2(c) is presented in Fig.3.

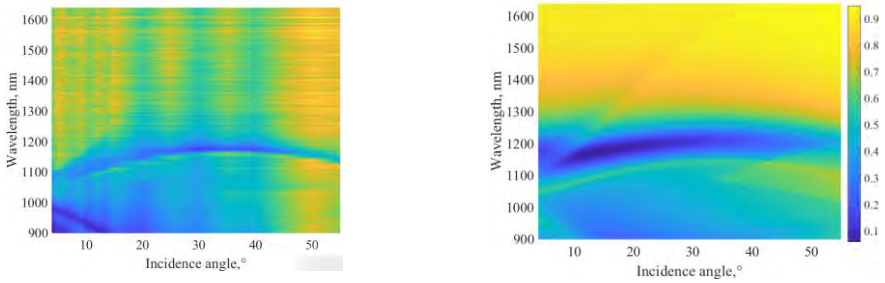



(a) (b) (c)

Fig.3. (a) – two expositions with angle 60° between them produce hexagonal pattern of energy density distribution (exposition time 160 s, laser power ~225 μW/cm$^2$); (b) – sensitivity curve of photoresist S1805; (c) – calculated grating topography based on (a) and (b) for development time ~9s (to be compared with AFM image fig2(c)).

## 4. REFLECTION MEASUREMENTS

Good accordance was found between the modeled and measured angle-resolved reflection map for the example of fig.2(c):




(a) (b)

Fig.4. Measured (a) and calculated (b) zero-order reflection map for the grating of fig.2(c).

The measurements of zero reflection order were made by spectrometer NIRQuest 512. The simulation was performed using MC grating package [10] based on RCWA method. On both pictures of Fig.4 three plasmonic lines are clearly visible, corresponding to plasmon coupling with different 1$^{st}$ diffractive orders: (0,1) and (1,0) for lower line; (0,-1) and (-1,0) for intermediate line; (-1,-1) for upper line.

## 5. CONCLUSION

To conclude we experimentally demonstrated the possibility of laser interference lithography to produce 2D gratings with essentially different topographies – from holes to pillars – using the same photoresist. To simplify the design of such structures we modeled exposition and development processes with real parameters of the lithography setup and the photoresist. Good accordance between calculated and real topographies is proven directly by AFM data and indirectly by comparison of experimental and theoretical angle-resolved reflection maps. Using such approach interesting plasmonic effects (like a strong dependence of plasmonic resonances on structure fill factor and height) that are not yet fully understood for 2D case can be efficiently analyzed theoretically and observed experimentally.

## ACKNOWLEDGMENTS

The authors thank Jean Yves Michalon from Hubert Curien laboratory for the metal layer deposition.

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## Electron-Beam Lithography and Two-Photon Polymerization for enhanced nano-channels in network-based biocomputation devices

**Danny Reuter[a], Sönke Steenhusen[b], Christoph Meinecke[c], Georg Heldt[a], Matteo Groß[b], Gerhard Domann[b], Till Korten[d], Stefan E. Schulz[a]**

[a]Fraunhofer ENAS, Technologiecampus 3, 09126 Chemnitz, Germany
[b]Fraunhofer ISC, Neunerplatz 2, 97082 Würzburg, Germany
[c]Technische Universität Chemnitz, Center for Microtechnologies, Reichenhainer Str. 70, 09126 Chemnitz
[d]Technische Universität Dresden, B CUBE – Center for Molecular Bioengineering and Center for Advancing Electronics Dresden, Arnoldstraße 18, 01307 Dresden, Germany

A vast number of combinatorial problems, such as the design of circuits, protein folding, and optimal network routing, are inaccessible for conventional computers due to their inherently complex nature. One solution to deal with this is to highly parallelize computations and to explore new technological approaches beyond semiconductor-based computers. Parallel computing by using biological molecules in networks is such an approach, which could solve these problems more efficiently [1].

The presented biocomputational approach uses a combination of physical and chemical guiding of filaments by biomolecular motors. For this purpose, state-of-the-art e-beam lithography (EBL) enables the fabrication of large area nanostructured channels with a typical channel width of 200 nm. These channels are functionalized by the immobilization of kinesin molecules as molecular motors to guide the filaments unidirectionally along the lithographically defined channels. The nano-channel network consists of different junctions, which represent the mathematical operations, the interconnections between these junctions, exits and landing zones for the filaments to get in touch with the molecular motors. An example of such a biocomputational network can be seen in Figure 1. Details of the fabrication technology have already been published [2]. This biocomputational network is a two dimensional (2D) network of $SiO_2$ channels, with an Au “floor” at the channel bottom only, forming the system of hierarchical structured junctions. The structures were fabricated on a silicon wafer with a 100 nm thick sputter-deposited Au layer that is sandwiched between two Cr adhesion layers. Next, a 500 nm thick $SiO_2$ layer was deposited by PECVD, followed by a Cr layer – acting as a hard mask during plasma etch. This Cr layer was patterned by reactive ion etching using a PMMA layer which was nano-patterned by e-beam lithography. The $SiO_2$ nano-channels were opened using an ICP Oxford Plasmalab System. In a final process step remaining resist residues and the Cr hard mask were removed in a dry etch process.

Despite the tremendous capabilities of the 2D nano-channel system for solving computational problems the architecture of the junctions can cause problems, especially in the pass junctions. Here the filaments are supposed to pass without any interaction with others and particularly without taking wrong turns. It turned out, that there are finite error rates, leading to wrong solutions of the mathematical problem [1]. Particularly for scaling up the 2D nano-channel networks, cutting down the error rates in pass junctions is essential for the device functionality.

For this reason we investigate the fabrication of so-called “error free junctions” (EFJs) that separate the pathways of filaments by going into the third dimension. The concept is to manufacture a combination of bridges and tunnels for entire avoidance of any contact between crossing filaments. The technology we employ for the generation of these complex 3D shapes is two-photon polymerization (2PP). In 2PP femtosecond laser pulses are tightly focused into a photopolymer. Inside the focal volume the light intensity is extremely high which enables the simultaneous absorption of two photons. Hence, a solidification of the material that is strongly confined to the focal volume is possible. This can be exploited to create arbitrary structures in 3D space in a layer-by-layer fashion very similar to conventional 3D printing with feature sizes down to 100 nm.

The design for an EFJ is depicted in Figure 2 (a). Here, a rendering of the EFJ is shown together with the preparation of vector data (contour lines and filling vectors) for the fabrication process. In first

studies we optimized the fabrication parameters as well as the illumination strategy for different kinds of photopolymers (in our case inorganic-organic hybrid polymers – ORMOCER®s) on glass and silicon substrates. A typical example of a resulting EFJ is depicted in Figure 2 (b). For demonstration we fabricated a simple device with two reservoirs for the seeding of filaments which are connected by a single EFJ. The resulting channel width is approximately 1 µm. In the detailed view it can clearly be seen that there is a tunnel underneath the bridge, so that filaments can travel across the junction without any contact to the second path. This is also indicated in the height characterization depicted in the lower right-hand picture. In our contribution, we will discuss the fabrication of EFJs as well as critical parameters e.g. channel width and wall height.

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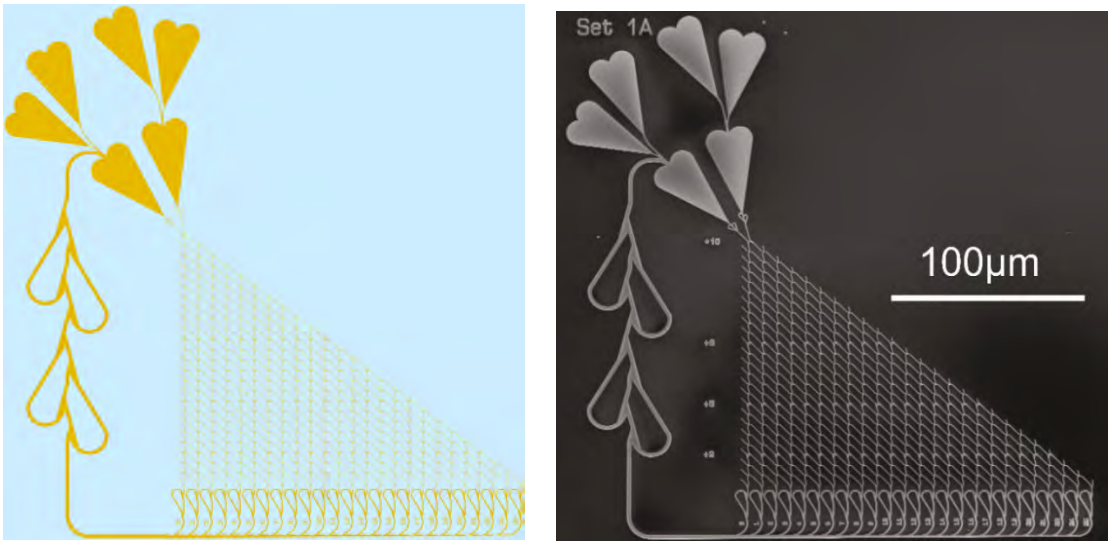


Figure 1 left: Network layout right: SEM image of the entire network after electron beam lithography.

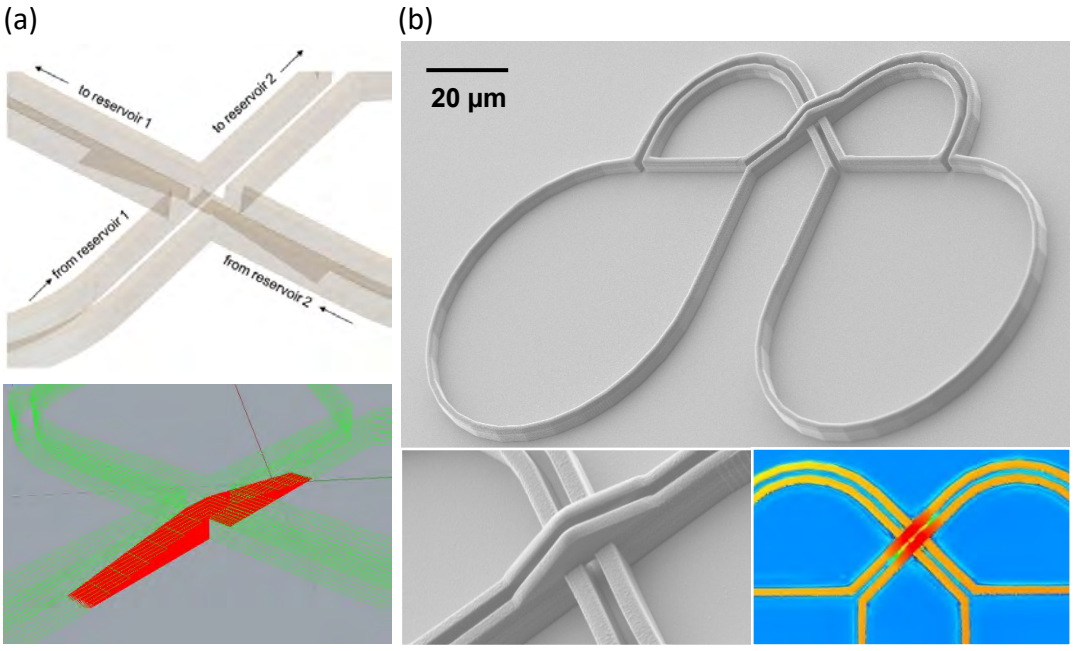


Figure 2: (a) Design of an error free junction. Upper image: Rendering of a detailed view. Lower Image: Contour vectors (green) and filling vectors (red) for 2PP fabrication. (b) SEM images of a fabricated demonstrator device with a detailed view and height characterization.

# Limits of model-based CD-SEM metrology

J. Belissard, J. Hazart
*CEA-LETI, 17 rue des Martyrs, Grenoble, France*
*jordan.belissard@cea.fr*

S. Labbé, F. Triki
*LJK, Université Grenoble Alpes, 700 avenue Centrale – Domaine Universitaire, Saint Martin d'Hères, France.*

Although the critical dimension (CD) is getting smaller following the ITRS roadmap, the scanning electron microscope (CD-SEM) is still the most general purpose tool used for non-destructive metrology in the semiconductor industry. However, we are now dealing with patterns dimensions in the same order of magnitude as the electron interaction volume and therefore, the usual edge-based metrology methods fail, because the edge effects are mixed up for sub 20 nm Si lines (see Figure 1).

Like scatterometry has extended the resolution of optical metrology through complex modeling of light-matter interaction, some electrons-matter simulation models[1] have been proposed. They could be used to improve accuracy and precision of CD-SEM metrology. However, these model-based approaches have their own fundamental limits mainly due to probe size with respect to the considered structure and noise. This paper analyses these limits assuming the model is perfect and the microscope has no systematic defect.

In this simulation study, we have used the model proposed by D. Nyyssonen[2], assuming to perfectly represent the SEM effects in the image. This model uses a precomputed diffusion matrix using JMONSEL software, developed by the NIST (National Institute of Standards and Technology). The D. Nyyssonen model is faster than Monte Carlo models, and it has less parameters than other compact models.
For computational reasons, we have limited ourselves to the one-dimension signal profiles. The feature of interest is limited to trapezoidal lines with various CD, sidewall angles (SWA) and heights (see Figure 2). We have carried out the study with several beam energies, tilts and probe sizes.

Sensitivity analysis shows surprisingly that with typical noise amplitude, even sidewall angle and height can be determined with a reasonable precision using top view SEM images (see Figure 3). Since these precision figures depend on the geometries, we provide useful tables giving the ultimate precision for various dimensions (CD, height, SWA).
More details will be discussed during the conference.

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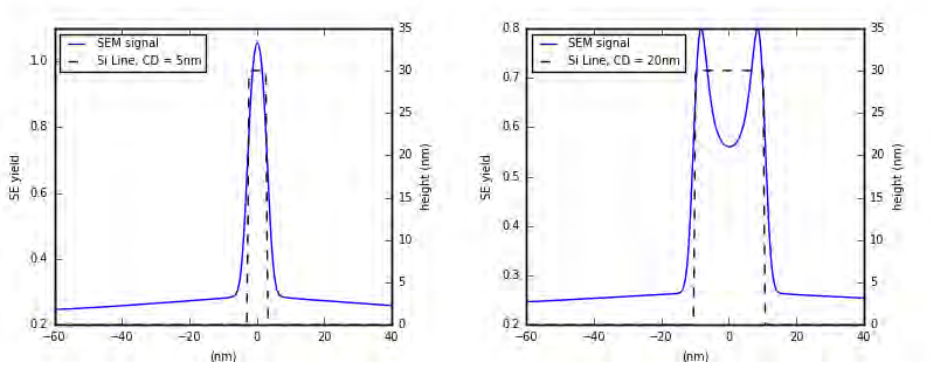


*Figure 1: Simulated SEM signals for two Si lines, with CD of 5 nm (left) and 20 nm (right).*

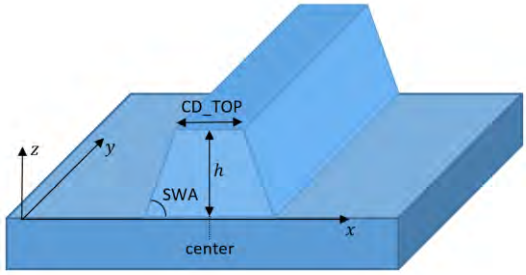


*Figure 2: Trapezoidal Line.* The line is defined by four parameters: the top CD (CD_TOP), the Sidewall Angle (SWA), the height (h) and the center of the line.

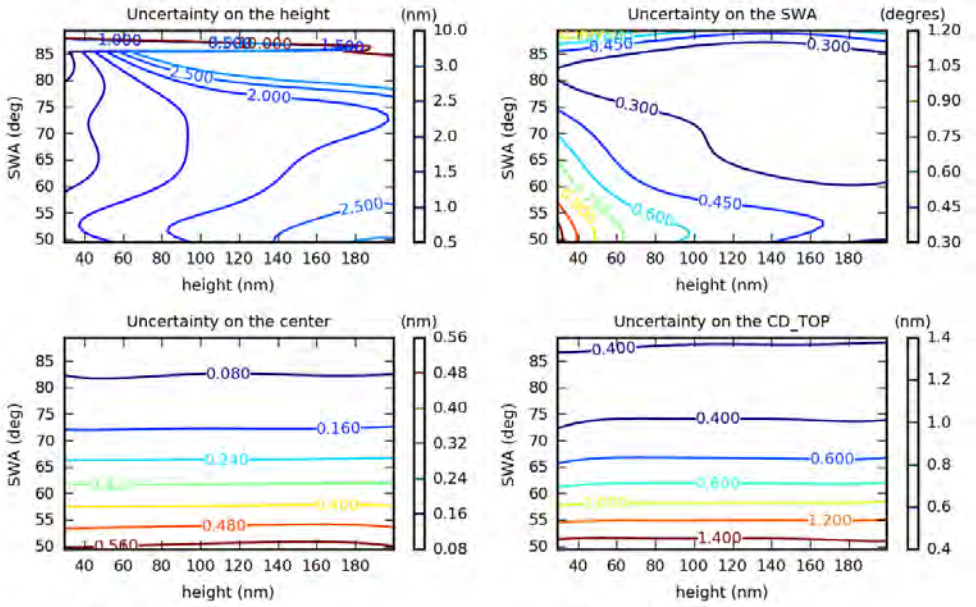


*Figure 3 : Uncertainty on parameters estimation as a function of the SWA and the height of the line*. The top CD of the line is 20 nm. The electron beam energy is 2500 eV, and the incidence is normal (zero tilt condition).

# Manufacturing of roughness standard samples based on ACF/PSD model programming

**Jérôme Reche[a,b], Maxime Besacier[b], Patrice Gergaud[a], Yoann Blancquaert[a]**

[a] Univ. Grenoble Alpes, CEA, LETI, DTSI, F-38000 Grenoble, France
[b] Univ. Grenoble Alpes, CNRS, CEA-LETI Minatec, LTM F-38054 Grenoble, France

Nowadays, in the microelectronic industry, Line Edge Roughness (LER) and Line Width Roughness (LWR) control presents a huge challenge for the lithography step. For advanced nodes, this morphological aspect reaches the same order of magnitude than the Critical Dimension, which leads to an increased power consumption by transistors and devices[1–5]. For example, the acceptable roughness for 10 nm node is 0.8 nm, and therefore the resolution of the measurement must be at angstrom scale. Hence, the control of roughness needs an adapted metrology. The current technique for CD analysis and roughness extraction is the Critical Dimension Scanning Electron Microscopy (CD-SEM). In case of roughness, it is based on the extraction of a Power Spectrum Density (PSD). After the edge detection, the Auto-Correlation Function (ACF) is used and the Fourier Transform (FT) is processed to obtain roughness information in frequency domain. Further, data noise can be removed and roughness parameter can be extracted[6].

A previous study[7] has shown PSD extraction performance with periodic lateral roughness (amplitude and frequency) along the line length. The current study proposes to manufacture samples closer to real case using programmed roughness based on a PSD model. These samples can be used as standard to evaluate capabilities of several tools. This kind of sample can also be considered as a part of the global methodology of roughness measurement for calibration of some techniques, for example scatterometry coupled with data learning process. This work covers the problems related to constraints of different methods. Indeed, nowadays, the technologies available for roughness measurement have several constraints like dimensions, material property and repeatability. The final standard samples are made compatible with the main metrology techniques, i.e. Atomic Force Microscopy, Scanning Electron Microscopy, Small-Angle X-ray Scattering and optical Scatterometry.

The work proposed here consists of four technical steps. The first step involves the creation of virtual layout with the programmed PSD. The PSD model (Equation 1) used here comes from the Auto-Correlation Function [6], which describe correlation between a signal and its copy shifted of *m* (Equation 2), and the Fourier Transform. With the use of random generation following normal distribution and inverse Fourier Transform ($FT^{-1}$), it is possible to generate signal variations. These variations correspond to the Line Width Roughness (LWR) or Line Edge Roughness (LER). Line shape can be constructed with addition of mean width value and pitch value. By repeating this method it is possible to obtain line gratings as shown in the Figure 1.a. The PSD model allows having a full description of roughness with three parameters: $\alpha$ the roughness factor, $\xi$ correlation length and $\sigma$ the standard deviation. Another important value in this study is $\Delta y$ the sampling along y, which corresponds to the resolution on this axis. An example of a visible sampling of 1 nm is shown in the Figure 1.b, which corresponds to a zoomed part of Figure 1.a.

The second step is the lithography one. In this work, gaussian e-beam lithography is used with Chemically Amplified Resist (CAR) in order to obtain a good pattern resolution and also to have the flexibility in creating different line gratings by varying $\alpha$, $\xi$ and $\sigma$. This step induces 'natural' roughness due to the tool and chemical interaction. In these conditions it is important to have a reference sample, without programmed roughness. With this strategy the impact of "natural" roughness can be removed of the further analysis[7]. Later on, silicon etching is done to obtain stable samples.

To ensure the quality of these standard samples, measurements are made with CD-SEM. 200 lines are measured per samples. A treatment involves the detection of edges along 2 µm length without filter are processed. These edges extracted are considered one by one in case of LER and two by two for LWR extraction. Further, a treatment corresponding to the Equation 1 is processed on the detected signal and the PSD of all the lines are averaged. Later, the PSD of reference sample (without programmed roughness) measured by CD-SEM is subtract (Figure 2) from PSD of programmed roughness measured by CD-SEM. The residual PSD are fitted to recover the three programmed roughness parameters: $\alpha$, $\xi$ and $\sigma$.

$$P_n = \frac{\Delta y}{2\pi N}\sigma^2\left[\sum_{m=0}^{N-1}(2-\delta_m)\; e^{-\left|\frac{m\Delta y}{\xi}\right|^{2\alpha}}\; cos(\,k_n m\Delta y)\,(N-m)\right]$$

Equation 1: PSD from ACF with three parameters fractal model,
α the roughness factor, ξ correlation length, σ the standard deviation
with N the number of points, Δy the sampling along y and $k_n$ the wavenumber

$$R(m) = \langle [w(y) - \langle w(y)\rangle\,][w(y+m) - \langle w(y)\rangle\,]\rangle$$

Equation 2: Autocorrelation function for stochastic process ω(y)

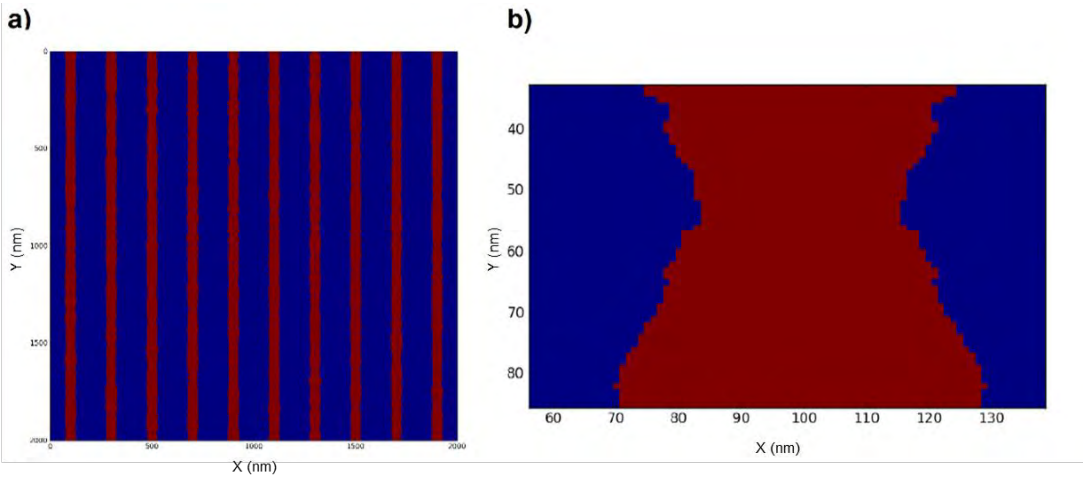


Figure 1 : Line gratings layout generated a) 10 lines, pitch of 200 nm, CD 50 nm
b) Zoom of the gratings where sampling is visible (1 nm)

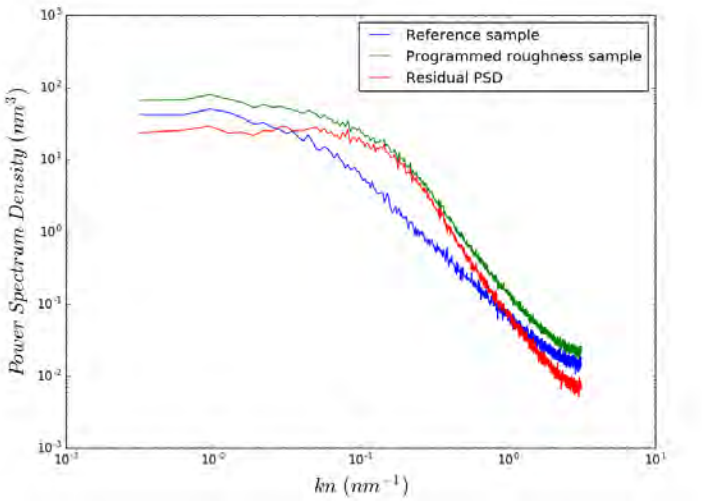


Figure 2: PSD extraction from the reference sample (blue) and the programmed sample (green),
and the residual PSD (red = green – blue)

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# Research on Data Augmentation for Lithography Hotspot Detection Using Deep Learning

Vadim Borisov[a] and Jürgen Scheible[a]

[a]Robert Bosch Center for Power Electronics, Reutlingen University, Reutlingen, Germany

**Keywords:** Lithography, lithography hotspot detection, deep learning, data augmentation.

## ABSTRACT

The hotspot detection has received much attention in the recent years due to a substantial mismatch between lithography wavelength and semiconductor technology feature size. This mismatch causes diffraction when transferring the layout from design onto a silicon wafer. As a result, open or short circuits (i.e., lithography hotspots Fig.1) are more likely to be produced.

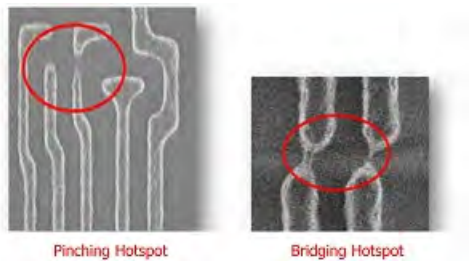
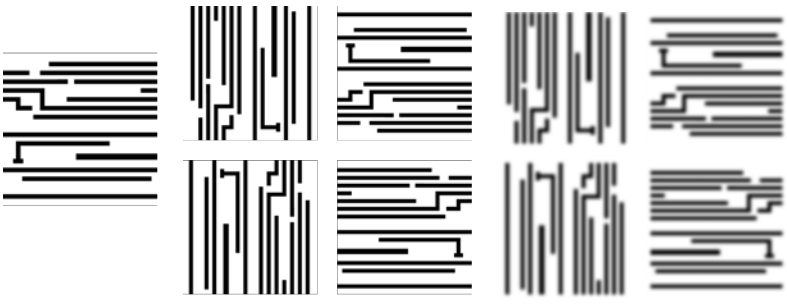



Figure 1. SEM images of two types of lithography hotspots.[1]

Nowadays, the state-of-the-art solutions for the lithography hotspot detection are principally based on machine learning (ML) and particularly on deep learning (DL) methods.[2–5] The most critical element for any ML or DL systems is training and test data.[6] Due to its nature, train and test data for the lithography hotspot detection problems are highly imbalanced, e.g. the ICCAD'12 dataset[7] contains less than 7% files with hotspots. In this situation, most of the ML and DL classifiers are biased towards the major class and hence show poor classification rates on a minor class.[6] The primary practice for overcoming the data imbalance is - *data augmentation*.



(a) (b) (c)

Figure 2. Example of DA: (a) original mask layout, (b) Rotation DA, (c) Gaussian (Blularization) DA.

Data augmentation (DA) is a method which refers to the process of creating new similar samples to the training set, thereby help to reduce the gap between classes. DA is used not only for DL methods, it also helps traditional ML and not-ML based hotspot detection algorithms.[8] However, to best of our knowledge, there is no

work study attending to compare and analyze different data augmentation techniques in term of the lithography hotspot detection data.

In this work, we explore the impact of various data augmentation methods (Flipping, Shifting, PCA jittering, Noise, Rotation, Random distortions, Tilt augmentations, and Skew augmentations) on the lithography hotspot classification task using Convolution Neural Networks (CNNs). The architecture of the used network is presented on Fig. 3.

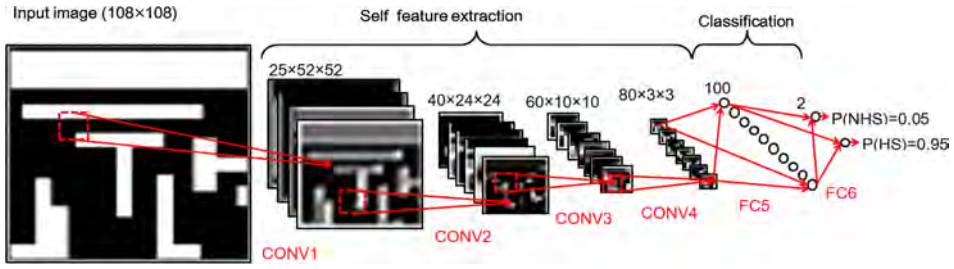



Figure 3. Architecture of the CNN model, which consists of several CNN layers and two fully-connected layers at the end.[5]

The main contributions of this work to the field are:

- We compare and analyze various exiting DA methods for the lithography hotspot detection problem;
- We present new lithography hotspot detection related methods for the DA. Our findings demonstrated that the proposed methods are particularly effective for improving prediction accuracy in small and imbalanced datasets.
- We propose novel DA methods for the lithography hotspot classification or detection.

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# Silicon Photonics : from research to industrial reality
(Keynote)

**Frederic Boeuf**

Silicon Photonics Technologies Manager

**STMicroelectronics**

Crolles, France

In the last 10 years, the development of modern society lead to an increasing need for transferring large amount of data. This amount is doubling every 18 months. As a consequence, the need for high-speed, low power and low cost interconnects is increasing. Traditionally optics was preferred for the long distance and high-speed transmissions due its lower power consumptions than the Cu-wire-based transmission. Nevertheless, the development of hyperscale datacenters lead to a need of shorter reach optical interconnects, and in the future high performance computing will also request ultra-high-bandwidth on ultra-short reach. Therefore some high-volume and low cost solution must be found. During the 1980's, researchers started to think about optical system relying on the same technology as CMOS chips: silicon material. Indeed, Silicon is transparent in the 1.3-1.5µm wavelength range used in telecom and datacom, and the optical refractive index contrast between Si (3.5) and SiO2 (1.5) is much higher than in glass-based technologies and even InP platform, allowing the fabrication of ultra-compact circuits on SOI wafers. With this in mind, between 1990's and 2010's, researchers demonstrated all the basic building blocks necessary to build an optical device library with Silicon. In this paper we will give on overview of main markets for Silicon Photonics, describe a 300mm wafer based industrial technology and finally discuss on the weaknesses of the Silicon photonics integration and what would be the future evolutions.

# Lithography technology and trends for More than Moore devices
## *Advanced Packaging & MEMS devices*

Amandine PIZZAGALLI
Yole Développement
75 Cours Emile Zola, 69100, Villeurbanne - Lyon, France
Phone: +33 4 72 83 01 00, pizzagalli@yole.fr

### Biography

Amandine Pizzagalli is in charge of equipment & material fields for the Semiconductor Manufacturing team at Yole Développement after graduating as an engineer in Electronics, with a specialization in Semiconductors and Nano Electronics Technologies. She worked in the past for Air Liquide with an emphasis on CVD and ALD processes for semiconductor applications.

### Abstract

Lithography requirements for Advanced Packaging & MEMS are very different compared to mainstream semiconductor industries' needs. Even if the market entry barrier is much lower in the "More than Moore" market, customer adoptions needs are higher in the packaging area with respect to resolution, overlay, sidewall angle, and depth of focus (DOF), wafer handling for wafer bow and backside alignment.
Key technical trends, requirements and challenges regarding the lithography technologies will be addressed in this paper.
In addition, more insights on the current and emerging lithography methods for More than Moore devices will be included, as well as market forecast, competitive landscape of the major equipment suppliers addressing these fields.

***Keywords—Lithography, resolution, RDL, wafer warpage, Depth of Focus (DOF), Advanced Packaging, MEMS, More than Moore***

### Introduction

The photolithography market for Advanced Packaging & MEMS is very different compared to the "More Moore" or mainstream semiconductor industry and exhibits very complex technical specifications. Indeed, customer adoptions requirements are much higher in the packaging area as well as MEMS & Sensors devices with respect to resolution, overlay, sidewall angle, and depth of focus (DOF), wafer handling for wafer bow and backside alignment. Resolution required in the front-end differs from the resolution required for Advanced Packaging which is in the single digit micron range. The current minimum resolution requested is below 5 µm for some advanced packaging platforms, like 3D integrated circuits, 2.5D interposers, and wafer level chip scale packaging (WLCSP). A lot of development is being made to reduce overlay issues due to shifting dies and obtain vertical sidewalls for flip-chip and WLCSP. In addition, higher DOF in a range of 10 µm is needed to handle thicker resists as well as high wafer topography. High DOF is also needed for MEMS projection systems and for some MEMS devices including DRIE steps with high resist thickness.

### Lithography technologies trends for Advanced Packaging & MEMS devices

Advanced Packaging has very complex technical specifications which differ from those associated in the front-end area.
Warpage handling as well as heterogeneous materials represent big challenges to photolithography. Due to aggressive resolution targets in Advanced Packaging, performance must be improved.
In addition, accurate layer-to-layer alignment is required for some MEMS manufacturing devices where misalignment features can lead to lower performance such as gyroscopes and micro-mirrors. Similarly, high DOF is required for projection systems and MEMS applications where high resist thickness is needed to enable DRIE process steps.

In the case of Advanced Packaging, stepper and mask aligners are today the two main lithography technologies used in high volume manufacturing. Mask aligners offer full wafer exposure and can process wafers very quickly. They have small throughput advantage and are the cheapest process compared to other lithography technologies. However, the systems have overlay limitations as they cannot handle distortion and die shift which need to be addressed for some Advanced Packaging platforms. On the other side, steppers are much more expensive but they have the ability to pattern small features at a resolution close to 2 µm with the best overlay. Thus, from lithography technologies point of view, steppers are mandatory for TSV packaging since it is based on very tight pitch between bumps with future needs of 20 µm micro-bumping capabilities. Bumps are scaled down to achieve better resolution for very high-level wiring density at the RDL level. General lithography requirements for TSV packaging are summarized in Figure 1.

Although mask aligner and stepper technologies are the most mature technology available on the market for Advanced Packaging,

new disruptive lithography technologies such as laser direct imaging (LDI) and laser ablation are also emerging and could contribute to market growth in coming years by offering adequate specifications at lower cost depending on the final application and requirements in terms of depth of focus (DOF), exposure field size, resolution and cost.
Significant business opportunities in the Advanced Packaging market are therefore driving photolithography equipment demand. Given the high growth rate of this market, there is no doubt that already established photolithography players and new entrants will be attracted.
In the case of MEMS devices, mask aligners represent the majority of brand new photolithography systems sold today. However, an increased market share for steppers is expected in the coming years to reach very accurate layer-to-layer. Nevertheless, due to its relaxed specs, the MEMS photolithography market benefits from a high percentage of re-used/retrofitted equipment coming from the mainstream front end semiconductor industry.

## Competitive landscape

The semiconductor industry is very often identified by its "More Moore" players, driven by technology downscaling and cost reduction. In the "More than Moore" industry the holy grail isn't downscaling any more – it's adding functionality. But it's still similar to photolithography.

The lithography market is technologically segmented with a significant gap between equipment suppliers in terms of resolution performance, cost coming from the front-end, and niche applications or back-end.

Front-end equipment vendors such as ASML and Canon provide the best tools in terms of resolution. However, they have limited DOF and therefore, are not suitable for Advanced
Packaging applications. In addition, they are typically much more expensive compared to the tools provided by specialized equipment vendors such as Veeco/Ultratech and SUSS MicroTec. On the other hand, back-end equipment is generally cheaper, but can face scaling issues as semiconductor ICs continue to shrink.

Equipment in the Advanced Packaging and MEMS industries is less complex but customer adoption needs are higher, which leads to a much broader photolithography landscape. As the photolithography market structure for these two industries is very different compared to the "More Moore", or mainstream semiconductor, industry, new entrants can penetrate these markets with a good knowledge of the technological building blocks.
Moreover, increased competition is driving acquisition between equipment vendors such as those between Veeco and Ultratech and KLA Tencor and Orbotech. These deals with help suppliers gain more value from the supply chain by capturing share in lithography equipment market.

Possible scenarios can happen including acquisitions, mergers, and joint ventures, along with their anticipated impact on the global photolithography market. Figure 2 presents some of the possible solutions that could happen in the future.

## Conclusions

Lithography for Advanced Packaging & MEMS devices is considered a market with a high potential for growth as it includes many different players along the supply chain. In addition, due to the different challenges to address in the lithography processes for Advanced Packaging & MEMS devices, there are huge business opportunities in those areas which could reshuffle the photolithography equipment demand to meet the requirements in terms of performances and cost.

## Illustrations

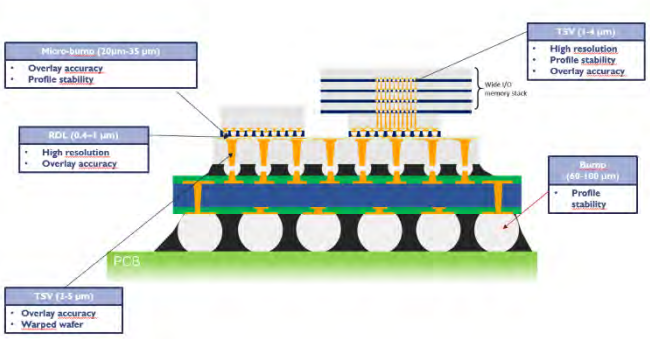


Fig.1. Lithography Requirements in Advanced packaging & MEMS

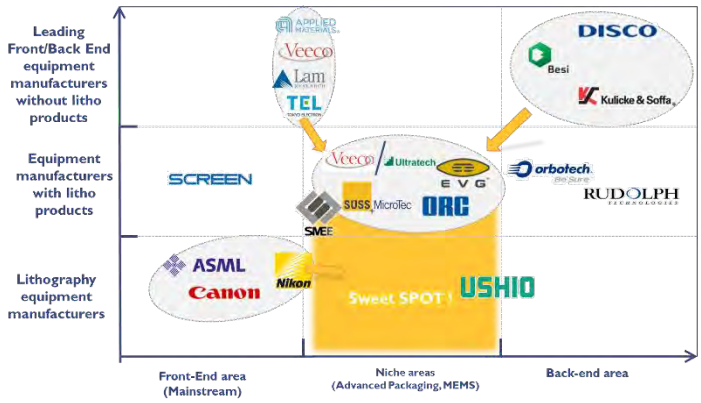


Fig. 2. Lithography player positioning: possible reshaping of the industry

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# Lithographic solution for yield detracting patterning defect signatures caused by Layout and Unit Process Recipe interaction

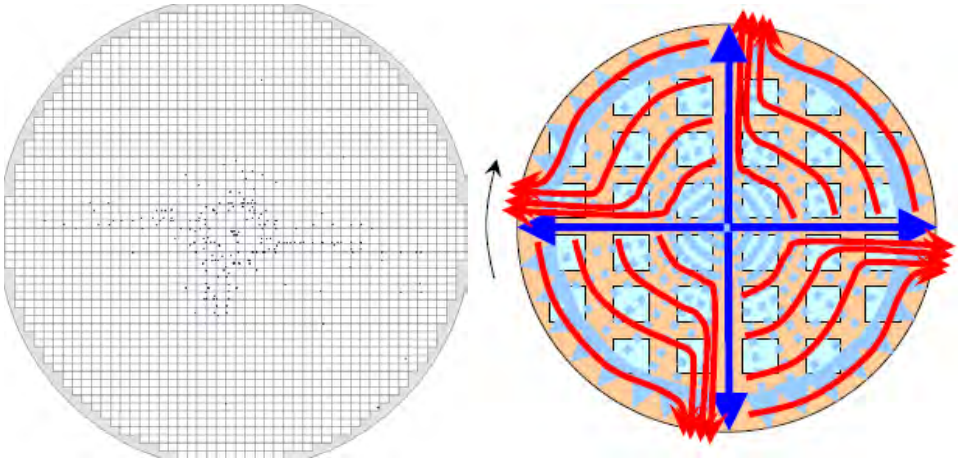
Matthias Voigt, Ronald Gaertner, Rolf Seltmann

GLOBALFOUNDRIES Dresden Module Two Limited Liability Company & Co. KG,
Wilschdorfer Landstr. 101, 01109 Dresden, Deutschland

## ABSTRACT

The 28nm process node is the last true single patterning node. Consequently, it is a low k1 (0.31) technology with nearly no design rule restrictions. To be cost effective and competitive, very high yields are needed. Yield loss can be separated into random (defectivity/particle driven) and systematic (process window driven) components. In lithography, the improvement of random defectivity primarily is concentrated toward improving the cleanliness of the photo chemicals by proper filtering and purging of the resist delivery line as well as optimizing the overall development and rinse recipes. This is a continuous, never ending process. On the other hand side, systematic, process window related fails are usually addressed in an early phase of the technology development by optimizing the OPC and the overall patterning process. In case of a none-perfect OPC it can happen that the process window for a specific hotspot is limited and barely is covering the overall variation budget. Such process window related fails usually are due to either a scanner mal-function, a none-perfect focus set-point, a bad mask, bad wafer planarity or local topography etc..

This investigation is about concentrating on a new defect type that is related to an interaction of specific layout configurations with the unit process development recipes. A simple example of such an interaction is the well-known “windmill” pattern. Depending from the hydrophobic characteristic of different surfaces post development residues occur (a).

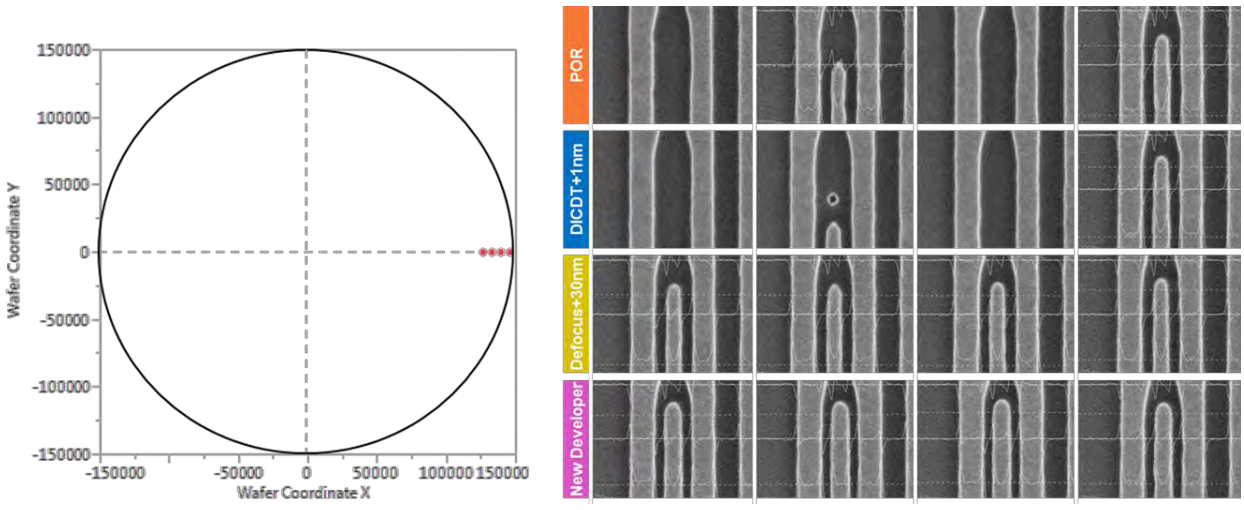


a) Windmill Defect Pattern b) DI Wafer Flow Orientation “with courtesy of Tokyo Electron Ltd.”

The shown water flow orientation in (b) during rinse process is more or less defined by layout, wafer topography and various recipe parameters. As a result a defect mechanism with a regional distribution can be observed.

As stated before very high yields are needed to be competitive. Specific extra pattern defects in the metal layers have been identified as a major yield detractor from a yield pareto. A cross functional team together with material and tool suppliers was formed to address this issue. As a result customized Developer Recipes were established leading to a yield gain of up to 0.2% per mask layer. This improvement can be divided in 2 major contributions, on the one hand random defectivity, on the other hand local wafer signature yield improvement. In dependency of Layout and Developer Recipe characteristics a well reproducible defect mechanism where a specific, critical device pattern failed at a certain location on the wafer has been observed. The fail occurs in a horizontal chain over multiple chiplets partially across neighboring shots, always at exactly the same location of the chiplets.

In a first step of troubleshooting, we did the usual process window check by varying dose and focus (c) i-iii). Looking into different DICD Targets did not improve the observed defect mechanism significantly. As the determined Focus threshold of +30nm cannot be supported by available Process Window, we looked into interactions of local parameters such as Wafer Location (Centre-Edge), Recipe Parameters, Topography, Orientation and more global predetermined parameters such as Design, homogeneous Pattern Density, OPC design, Weakpoints and Stack differences to improve this pattern failure. Consequently customized Developer Recipes had been created to fix the specific patterning problems (c) iv).




c) Post Polish Weakpoint Patterning at 4 neighboring 3o'clock DIEs. Impact of process changes (from top to bottom): i) POR; ii) within Process Window DICD Change +1nm; iii) out-of Process Window Defocus +30nm; iv) Tuned Developer Recipe

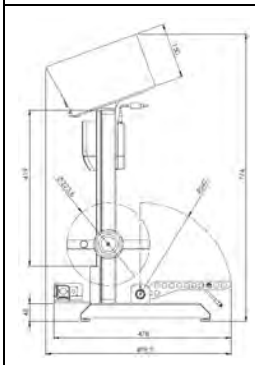
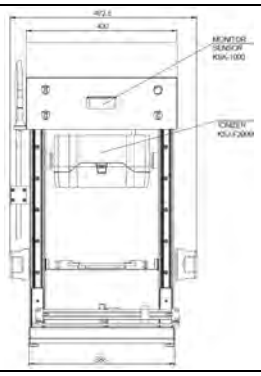
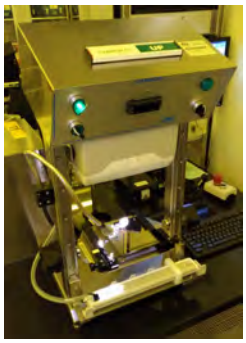
Beside the described physical parameter changes a further but more theoretical approach to resolve the observed defects was looking into chemical interactions such as the developer media which contains beside TMAH also specific surfactants.

# CK-MASK semi-manual tool for mask inspection and blowing

Andrea Leserri, Umberto Iessi, Francesco Ferrario
ST Microelectronics, Agrate AG8/MEMS Operation, Photo-Litho module

Photolithography masks require a periodical inspection and cleaning.
The visual inspection is often paired with a mask air blowing to remove eye visible particles.
If these steps are run manually they are really critical for mask integrity in terms of contaminations, scratches, fingerprints, pellicle damage.
All these potential issues arise during the mask certification process causing mask repelliculization, and, in the worst case, mask scrap with drawbacks linked to production aspects: quality (repetitive defects), cost (mask repels/remake), production lots on hold, non-linear production WIP and non-respect of production commitments.
AG8-AGM photolithography engineering team in collaboration with “Gusmini attrezzature industriali” developed a tool called “CK-MASK” able to handle 6” masks and to reduce the risks connected to masks inspection and blowing.

*Table 1: Tool view*

| LEFT VIEW | FRONT VIEW | TOOL IMAGE |
|---|---|---|
|  |  |  |

**APPLICATION:**

- Mask handling in “safe mode” during mask certification procedure → factory environment without automatic inspection tools capability
- Back-up for automatic inspection tools

The main aim of CK-MASK come from this critical balance in order to find a way to reduce at minimum level all manual steps involved in mask certification procedure and, as consequence, reduce the probability of mask damage/contaminations.
CK-MASK is basically composed by:

- Mask-Holder
- Ionized air-knife
- Ionizer
- Bright-light source
- Voltage sensor head

**SPECIAL FEATURES:**

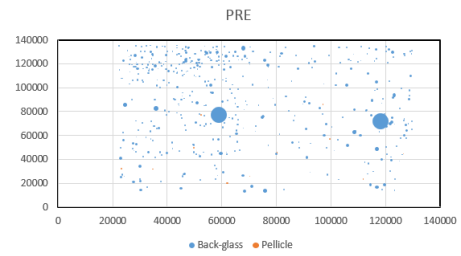
- all tool parts, in contact with the mask and subject to motion during tool utilization, have been built with **anti-wear materials**

- CK-MASK must be designed in order to reduce at minimum level the probability to cause ESD issue on masks:
  - All handling parts in contact with mask, and the parts directly connected to them, must be made with **conductive materials**
  - Whole tools must be **ground connected**
  - flow used to perform blow step (remove particles mechanically through flow pressure) must be **ionized**

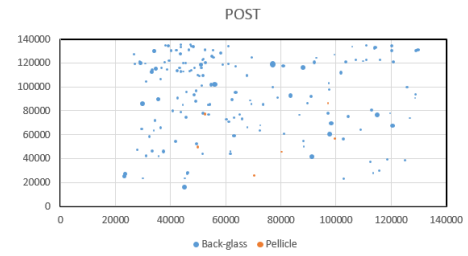
**TOOL QUALIFICATION** involved different steps:

- Particle contamination evaluation
- Cleaning efficiency (particle removal through blow step)

PRE




POST




| | BACK-GLASS | PELLICLE |
|---|---|---|
| PRE (#particle count) | 451 | 11 |
| POST (#particle count) | 161 | 6 |
| $\eta_{cleaning\ (\%)}$ | 64 | 45 |

- ESD prevention (voltage measurement pre vs post inspection on CKMASK)

CUG17BD300A1 (MASK SCRAPPED)

| | $V_{reference}$ [V] | $V_{post}$ [V] | $\Delta_{polarization}$ [V] |
|---|---|---|---|
| **Pellicle** | 6 | 20 | 14 |
| **Back-glass** | -4 | -10 | -6 |

CUG21AI830A1

| | $V_{reference}$ [V] | $V_{post}$ [V] | $\Delta_{polarization}$ [V] |
|---|---|---|---|
| **Pellicle** | -10 | 12 | 22 |
| **Back-glass** | 15 | -18 | -33 |

UM16BSF800B1

| | $V_{reference}$ [V] | $V_{post}$ [V] | $\Delta_{polarization}$ [V] |
|---|---|---|---|
| **Pellicle** | 7 | 10 | 3 |
| **Back-glass** | 13 | -10 | -23 |

UM55ASF105A1

| | $V_{reference}$ [V] | $V_{post}$ [V] | $\Delta_{polarization}$ [V] |
|---|---|---|---|
| **Pellicle** | 12 | 8 | -4 |
| **Back-glass** | 0 | -4 | -4 |

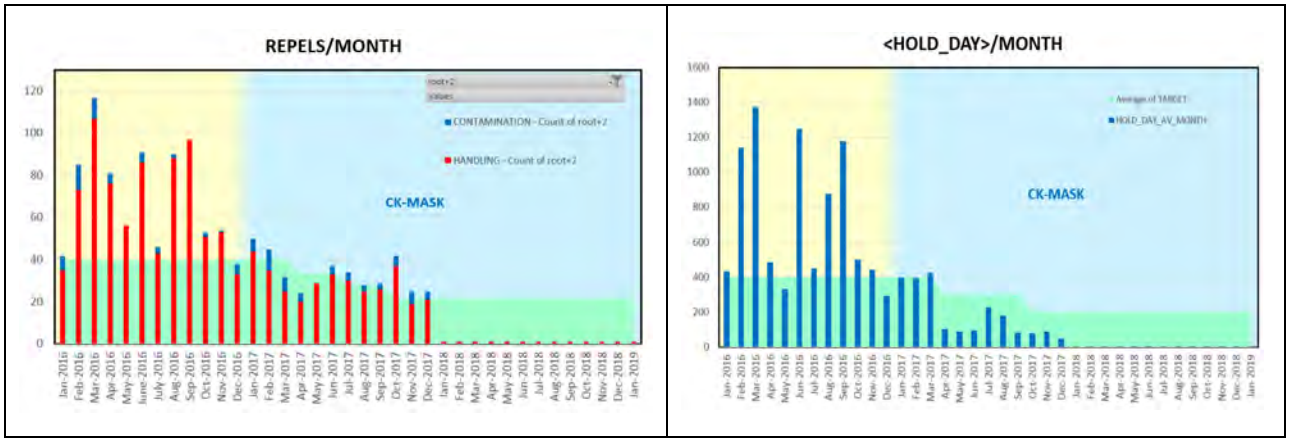
*Particle measurement for first and second qualification test reported above was done through PDS tool: POLLUX Dt.Shenk; voltage measurement for the third test was done through KEYENCE SK-050 sensor head.*

**CONCLUSION:**

CK-MASK tool was developed to minimize as much as possible all manual steps involved in the mask certification process, its deployment in production was successful as tracked by our main key indicators in Table 2: the mask repelliculization rate was almost halved and the average hold per day, due to mask unavailable for repelliculization for handling issues, was further reduced.

Lastly the investment request, respect to commercial available mask inspection tools, was strongly reduced (15KEuro vs 400KEuro).

*Table 2: Key indicators: Mask repelled and average wf on hold per day Trend monthly based (from Jan-2016)*



# The (almost) completely automated 12”-lithography

Jens Seyfert, Lars Albinus, Jens Arnold, Silvio Fritsche, Steffen Habel, Michael Mitrach and Mario Stephan
Infineon Technologies Dresden GmbH, Koenigsbrücker Str. 180, 01099 Dresden, Germany

## ABSTRACT

A fundamental aspect for the economic success of a semiconductor production is a low level of costs per wafer. A substantial part of these costs per wafer is accounted by personnel costs. For this reason, it is desirable to reach the lowest possible level of personnel costs. Mainly this is achieved by increasing the degree of the factory automation.

To increase the degree of factory automation, various approaches are conceivable and in use.

We were at the time the first 12”-fab worldwide and we were equipped with an OHT (Overhead Hoist Transfer) system of the first generation to transport to and load wafer pods on process equipment and wafer stockers. That means, that the complete wafer handling took place automatically. Viewed with a certain distance, the fab as a whole showed a high level of automation.

However, in the lithography it was necessary to handle reticles manually. Figure 1 shows the distribution between the automated wafer handling and the manual done parts reticle handling and necessary tool assist.

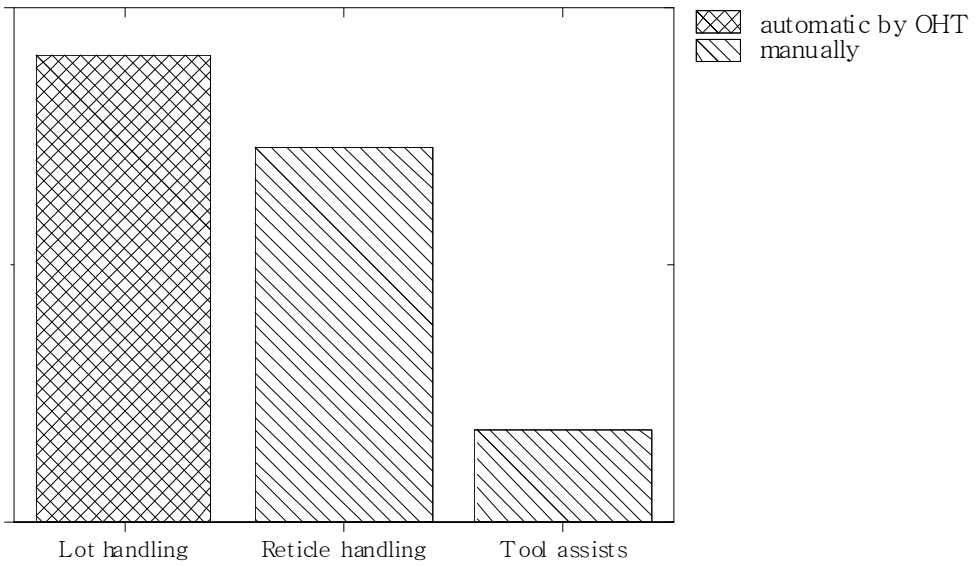



Figure 1: Estimation of the distribution of the fields of activity in lithography

The efforts for manual reticle handling and the resulting personnel costs contradicted the requirements of a highly automated manufacturing. An investigation about possible reticle automation scenarios by using AGV (Automated Guided Vehicles) or OHT to improve the

lithography automation level resulted in non-acceptable investments in relation to the saved personnel costs. As a result, further activities to automate reticle handling have been avoided.

But driven by the end of live situation of the used OHT system, a retrofit of the system in 2017 offered the possibility to install additionally to the lot OHT system a reticle OHT option. In conjunction with the findings of the above investigation, this new situation led to the decision to install this option to save the personnel costs of manual reticle handling.

Introductory in this paper, we would like to compare briefly conceivable automation scenarios by using AGV and OHT systems. We describe the advantages and disadvantages of both systems arising from our present situation. We justify why only the use of an OHT makes sense for us.

The main part of the paper is dedicated to the way from the ended OHT hardware startup to the running automated reticle handling.

First of all, we introduce the machinery used. The majority of the exposure equipment was not intended for OHT loading by tool manufacturer. We explain the modifications needed to allow a reticle loading of the exposure tools by OHT.

One key factor in getting the system up and running is the control of the exposure tools by host commands. These sequences are used to enable the tool operation without operator-tool interaction. Based on the reticle load and unload strategy, we explain basics of our used exposure tool control.

Another key factor is the system control algorithm. The whole reticle operation is controlled by a rule based dispatching system. The rules used combine robustness and necessary performance emphasizing the robustness of the system. The limitations of this rule based dispatching system are discussed and the use of a mathematical solver system recommended.

An important aspect of the introduction of the system is the fact that the exposure systems, the OHT and the reticle stockers were used to create a network of machines. This machine network requires functional monitoring approaches that are new to us. We consider possibilities to display status information of this complex network as simply as possible. The aim is to enable fast and efficient troubleshooting within the network.

Furthermore, this newly created machine network entails some intrinsic risks. The main risk of complete failure due to the failure of a sub component and ways to minimize this risk are discussed.

A summary of the practical experiences during the construction phase of several months completes the main part of this work.

It is expected that in continuous operation the demands on the performance and the robustness of the system will increase. In conclusion, we would like to point out possibilities for future system optimization. Based on the current state of knowledge and the implementation costs we will try to evaluate these.

Finally, we would like to comment on the title's restriction "almost". We explain why a completely automated lithography, which means including the additional automation of tool assists, is not possible from our current perspective.

# Fast local registration measurements for efficient e-beam writer qualification and correction

Klaus-Dieter Roeth, Hendrik Steigerwald, Runyuan Han, Oliver Ache, Frank Laske
(KLA-Tencor MIE GmbH, Germany)

Mask manufacturers are facing major reticle metrology challenges, driving the need for cost-effective solutions that provide tighter registration specifications and on-device registration qualification.

E-beam mask writers' local registration error may have a critical impact on the error contribution of the reticles to wafer overlay, as it is very local and most likely is not revealed with standard quality control schemes and sampling. The reticle error signatures are, of course, writing-strategy-dependent, but may also be caused by residual deflector alignment issues, thus leading to a very local but potentially critical non-correctable overlay error on the wafer. Since the e-beam writer strategy does not differ significantly between ArFi masks and EUV masks, we expect a similar error signature for both mask types.

We will present data which demonstrates local registration errors that can be correlated to the writing swathes of state-of-the-art e-beam writers and multi-pass strategies, potentially leading to systematic device registration errors versus design of close to 2nm. Furthermore, error signatures for local charging and process effects are indicated by local registration measurements resulting in systematic error, also on the order of 2nm.

A unique measurement methodology, Local Registration Metrology, is presented that allows for dense sampling of reticle dies to characterize the local e-beam registration error. Several thousand sites in a region of interest with length and width of a few hundred microns are measured. LMS IPRO metrology algorithms enable parallel registration measurement of all individual sites for fast and accurate metrology. High throughput allows completion of Local Registration measurement within a few minutes instead of exceeding a day of measurement time with conventional registration metrology strategies. This capability enables mask users to add local registration quality control to ensure the local wafer pattern placement error contribution by a mask is within the acceptable tolerance.

In addition, based on the results of Local Registration Metrology, e-beam mask writer corrections via feed forward can now be developed to significantly reduce local overlay error on wafer caused by the reticles.

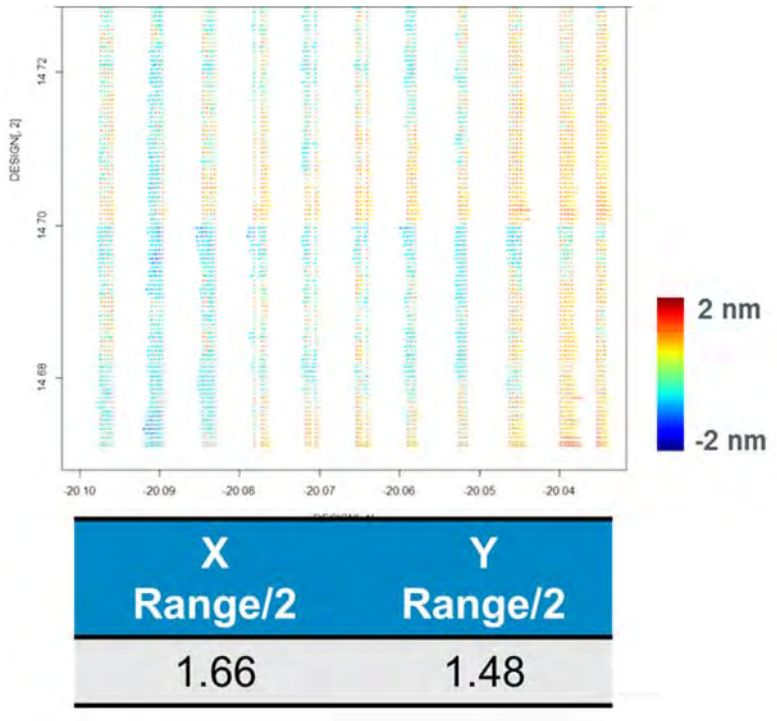



Figure: Dense, local registration map depicting the x-component of the registration error of a state-of-the-art e-beam mask writer in an area with width and height of ~80 µm. The range/2 for the whole die is 1.66 nm. The y-error is of the same order of magnitude.

Keywords: LMS IPRO, Metrology, Registration

# Failure analysis and prevention of patterning issues using OPC simulation and advanced method of contour analysis

Charlotte Beylier*, Frederic Robert, Benjamin Vianne,
STMicroelectronics, 850 Rue Jean Monnet, Crolles, France
*charlotte.beylier@st.com

## ABSTRACT

Optical Proximity Correction (OPC) verification during Mask Data Preparation (MDP) includes commercial Model Based (MB) and Rule Based (RB) solutions. In order to perform efficient mask verification, accurate models are necessary as well as calibrated detectors in order to catch patterning issues during OPC checks. This calibration requires multiple mask-silicon iterations and metrology cost to have pertinent correlation with patterning failures.

One limitation of current sign-off is that detection is applied on single layer lithographic simulation. The check is performed between contour of layer of interest and other designed layers, losing the gain of having interaction between contours. Stacking the contours is a more suitable way to mimic patterning issues and catch real failure risk. This work proposes to create 3D failure detection from stacked contours post-processing and analysis.

This work also proposes a solution for early failure detection and gives the opportunity of mitigating patterning issues during design conception. At STMicroelectronics, a platform named OFDEC (OPC For Design Check) has been developed which performs a DFM-oriented mask verification, and is a DTCO enabler. The output of the flow contains simulated contours and defects database highlighted by OPC verification.

In the framework of this study, an additional brick has been developed to enrich this platform with a contour post-processing module to go further in mask risk prevention. This module will be used as an advanced failure detection or analysis to address patterning risks that are not captured by the regular OPC sign-off. This module takes the very high added value of having all the layer contours and process variation band (PVB) in one database file.

By post-processing the contours, this module is able to take into account process contributions such as etch effects, epitaxy and overlay. Resist contours are distorted in order to have projection of 3D effects. The methodology of contour post-treatment calibration and verification will be explained.

A specific application on contact punch-through risk in C28FD-SOI technology is depicted in figure 1. In this figure, a real failure case highlighted in red shows that lithographic contours are not sufficient to discriminate the failed contact whereas 3D simulation is able to perfectly reproduce contact punch through phenomenon [1].

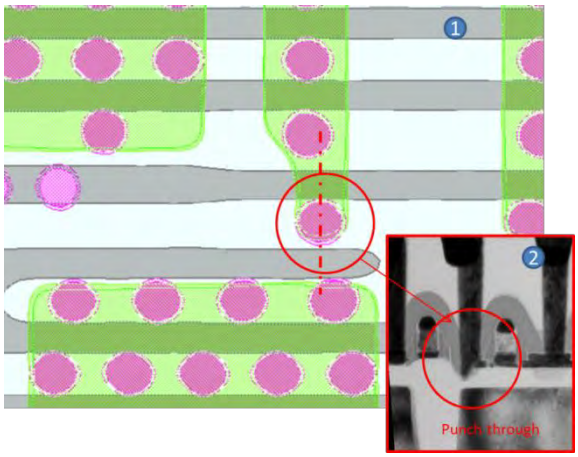



Figure 1: (1) layout of a punch through sensitive contact in QSRAM with active, poly and contact contours, (2) TEM cut of the sensitive contact.

With contour post-processing, the proposed method gives local emulation of 3D process effects to discriminate design configurations. In figure 2, the pattern 3D analysis shows green active contour at level 3 (figure 2b), representing post etch contour, is not significant to capture contact failure, whereas yellow active contour at level 2, representing epitaxy faceting contour is capturing contact under-enclosure.

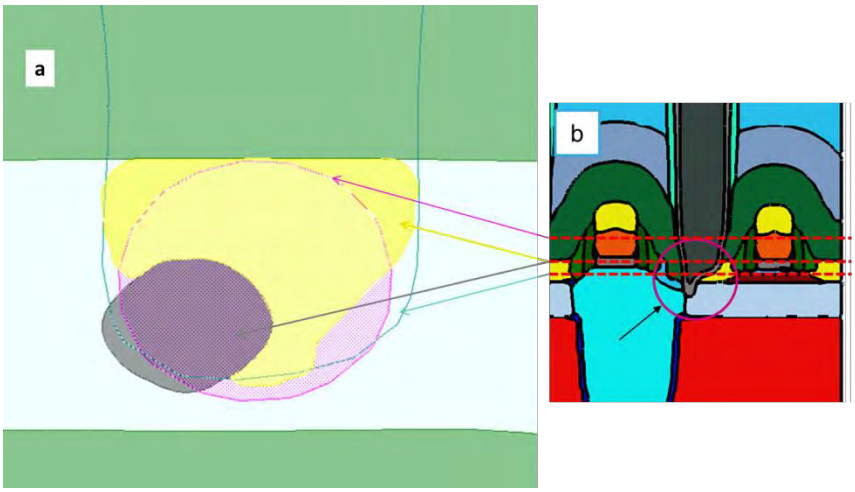



Figure 2: (a) contours post processed to emulate 3D effects. (b) 3D illustration of failure with 3 levels of contour extraction: 1, 2 and 3 (red dashed lines).

This work proposes an original approach to apply full chip detection that correlates silicon failure with pre-selected patterns. In that way customized detection can be applied on pattern families to increase detection accuracy and silicon correlation.

***Keywords: FD-SOI; failure analysis; Design-Technology Co-Optimisation; variability; OPC; contour analysis.***

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# Accurate determination of 3D PSF and resist effects in grayscale laser lithography

**Temitope Onanuga[a,b,c*], Corinna Kaspar[d], Holger Sailer[d], Andreas Erdmann[a,b,c]**
[a] Erlangen Graduate School in Advanced Optical Technologies (SAOT), Paul Gordan Strasse 6, 91052 Erlangen, Germany;
[b] Lehrstuhl für Elektronische Bauelemente (LEB), Cauerstrasse 6, 91058 Erlangen, Germany;
[c] Fraunhofer Institute for Integrated Systems and Device Technology, Schottkystrasse 10, 91058 Erlangen, Germany;
[d] Institut für Mikroelektronik Stuttgart (IMS CHIPS), Allmandring 30A, 70569 Stuttgart, Germany;

**Introduction:**

Laser grayscale lithography methods are increasingly applied in the fabrication of three-dimensional patterns such as optical gratings (Wilson et al. 2003), photonic couplers (Dilon et al. 2008), microfluidics and microelectromechanical devices (Falica et al. 2017). Many of these applications require a tight control of the 3D topography of the fabricated structure. However, due to the proximity effect, the designed dose distribution differs from the experimentally realized dose distribution, as the dose assigned to a particular resist pixel spreads out to neighboring pixels. Consequently, the desired topography is different from the intended topography. The dose distribution across pixels inside the resist for a single focused beam is known as the point spread function (PSF). In order to obtain the desired topography, the designed dose has to be corrected by considering the point spread function and other resist processes. This process of dose adaptation, known as proximity effect correction (PEC), is ubiquitous in grayscale processes (Unal et al. 2010). Fabrication of 3D structures with desired topographies in grayscale lithography therefore strongly relies on accurate determination of the PSF and model parameters of the resist processes.

The main achievement of this paper is showing that the 3D PSF and model parameters for the resist processes can be accurately determined from a comprehensive set of test patterns and a detailed model of the grayscale exposure process. In the following, we begin with a description of the test patterns and simulation models. Thereafter, we present a comparison of the developed test patterns to the best-fit simulated profile and demonstrate the model application to predict the topography of blazed gratings.

**Model description and test patterns:**

In grayscale laser lithography, the point spread function depends on the profile of the incident laser beam, the microscope objective and the wafer stack. As a first approximation, the PSF of grayscale lithography processes is commonly taken to be a Gaussian function with a fixed beam radius for all axial planes in the resist. We observed that this assumption results in a poor fit of experimental results and instead employ a double Gaussian model. The double Gaussian model better simulates the focusing of the incident Gaussian beam and back reflection that occurs at the resist-substrate interface. The resist processes are specified by modeling parameters that quantify light-resist and resist-developer interactions.

The 3D PSF and resist parameters can only be derived when test structures that encode such information are employed in the model calibration. Our test structures consist of a set of lines with varying line and background exposure doses. This array of test patterns closely relates to actual experimental patterns in which neighboring features typically have different dose values. By comparing the fabricated topography with the simulations, we obtained model parameter values that result in 3D simulated topographies, which most closely match the experimental topographies.

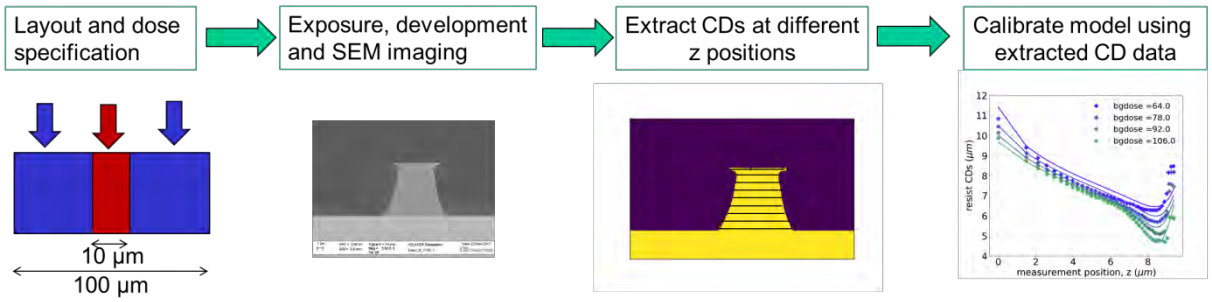


**Figure 1: Methodology applied in the determination of the 3D PSF and resist parameters. From left to right: specification of the dose distribution in the layout; measured SEM image after exposure and development; pre-processed SEM image to enable CD measurements; and a plot of the resist CDs versus the measurement position.**

Figure 1 presents the methodology applied in the determination of the 3D PSF and resist parameters. The test patterns consists of an array of lines with exposure dose varying from 0 to 45 a.u (colored red), while the background of the lines (colored blue) were exposed with higher doses varying from 64 to 106 a.u (Kaspar et al. ). For a positive-tone DNQ-type resist, used in this paper, the dose distribution results in a 3D line pattern at the center with a tail encroaching into the background. After exposure and development, we measured the cross-section SEM images using a conventional SEM ('Leo 1560'). The resulting SEM images were processed using standard image processing routines and their contours were extracted. With this, we obtained the CDs at different axial positions in the resist. The extracted CDs of the test patterns were then used to calibrate our PSF and resist model.

## Model fitting to experimental results:

Using a genetic algorithm, we found the model parameters for the PSF and the resist that best fit the simulated profile to the experimental profiles. The model parameters were fitted using the experimental results for dose equal to 0 and 40 a.u. The resulting best-fit parameters were then applied (without any other adjustments) to simulate doses of 10, 20, 30 a.u (results for 10, 30 a.u are not displayed).

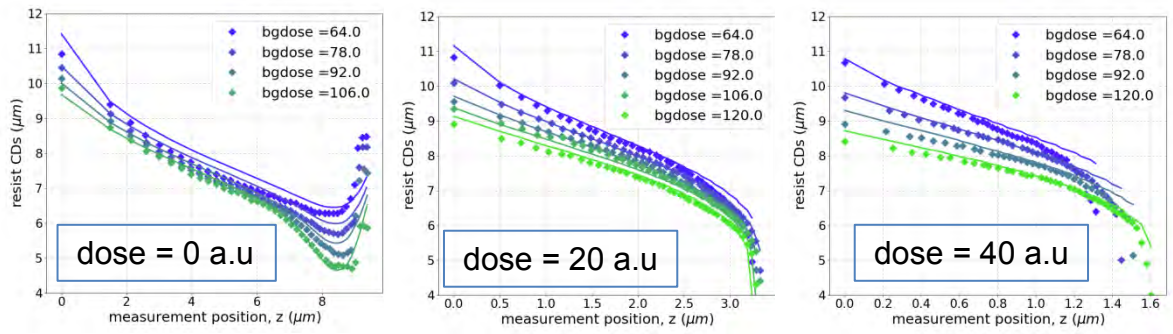


**Figure 2: Fit of resist CDs versus the measurement position. Each subplot corresponds to a particular dose level. Within each subplot are curves that correspond to the applied background dose. The experimental measurements are shown as markers on the plots while the simulations are the curves.**

Fig. 2 presents a plot of the experimental measured CDs and best-fit simulated CDs versus the z position. A zero measurement position on the horizontal axis corresponds to the resist-silicon interface. Each of the subplots exhibits the results for an exposure using a line dose of 0, 20 and 40 a.u (from left to right). The curves within each of the subplots represent a change in the background dose from 64 to 106 a.u. These simulation results were close to the obtained experimental results, indicating that the developed model is a good representation of the experimental process.

To verify the correctness of our model on a real-world application, we exposed a sawtooth pattern and compared the experimentally realized 3D topology with model predictions. The sawtooth patterns were fabricated on the same wafer as the test patterns (Fig.1 and Fig.2) so that an identical resist processing can be assumed for both patterns. The sawtooth patterns have pitches of 5.0 and 10.0 microns.
Fig.3 shows a cross-section cut through the sawtooth patterns and the related simulation results. The plots show that the experimental results were close to the simulation results for both pitches.

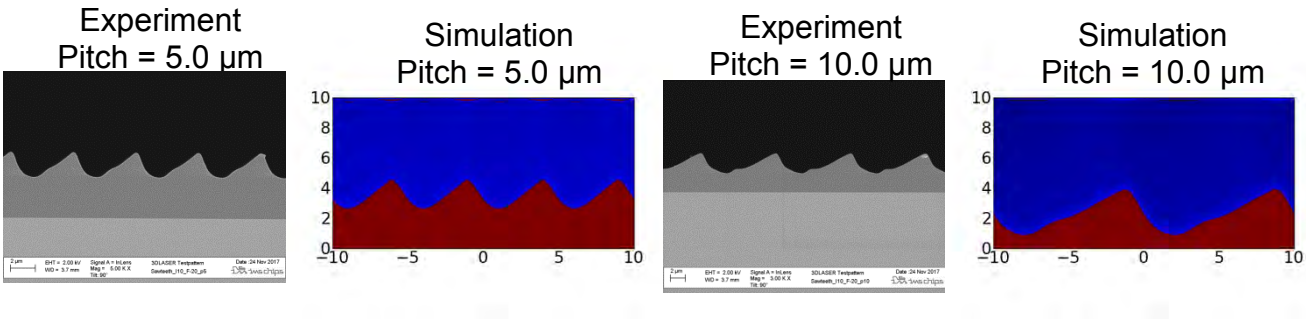


**Figure 3: SEM image and simulated profile of sawtooth patterns. The patterns have a pitch of 5.0 and 10.0 microns. The simulated profiles closely match the corresponding experimental profiles.**

## Summary and Outlook:

This paper presents a method to accurately calibrate a laser grayscale process. By combining a double Gaussian PSF and a detailed resist model, we could fit well the 3D topographies of selected test patterns. The obtained calibrated model was tested by comparing SEM images of fabricated sawtooth patterns with simulated sawtooth patterns. The simulated profile closely matches the experimental profile.
Having developed a robust model for the grayscale process, the obtained 3D point spread function and resist parameters can be employed in a more accurate proximity correction algorithm.

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# Photonic IC Lithography Software - Challenges and Solutions

Nezih Ünal[a], Ulrich Hofmann[a], Jens Bolten[b], Thorsten Wahlbrink[b] Anna Lena Giesecke[b], and Michael Hornung[b] , Jeroen Bolk[c],

[a] GenISys GmbH, Eschenstr. 66, 82024 Taufkirchen (Munich), Germany;
[b] AMO GmbH, AMICA,
Otto-Blumenthal-Straße 25,52074 Aachen, Germany;
[c] Eindhoven University of Technology, NanoLab@TU/e
De Zaale, 5612 AJ Eindhoven, The Netherlands

## ABSTRACT

Photonic applications are transitioning from R&D (device and process development) to production, with electron beam lithography still being one of the most widely used patterning technologies. The use of conventional CMOS technology for the fabrication of photonic circuits poses interesting challenges, as design characteristics (curved vs. Manhattan layouts) and lithography requirements (feature fidelity and minimum LER vs. CD control) are quite different between photonic devices and standard CMOS. These challenges are visible in the entire design flow, from the design domain (with EDA startups focusing on photonic designs) to tape-out (fracturing to minimize LER is very different from fracturing to get uniform CD distributions) and manufacturability (OPC and DRC). CMOS paradigms such as “a vertex describes design intent” will have to change as the digitization of curves is design tool dependent and are not useful as a metric for design intent. Moreover, with the transfer of photonic IC’s from R&D to production it will be required to transfer the processes to optical lithography, requiring changes in standard resolution enhancement techniques. As OPC today is optimized for CD control, it will have to adapt to different quality criteria such as feature fidelity and minimal LER.

In this paper we will discuss the special requirements of data preparation for photonic applications in e-beam lithography and the transfer to optical lithography with the challenges of OPC and MDP for photonic designs.

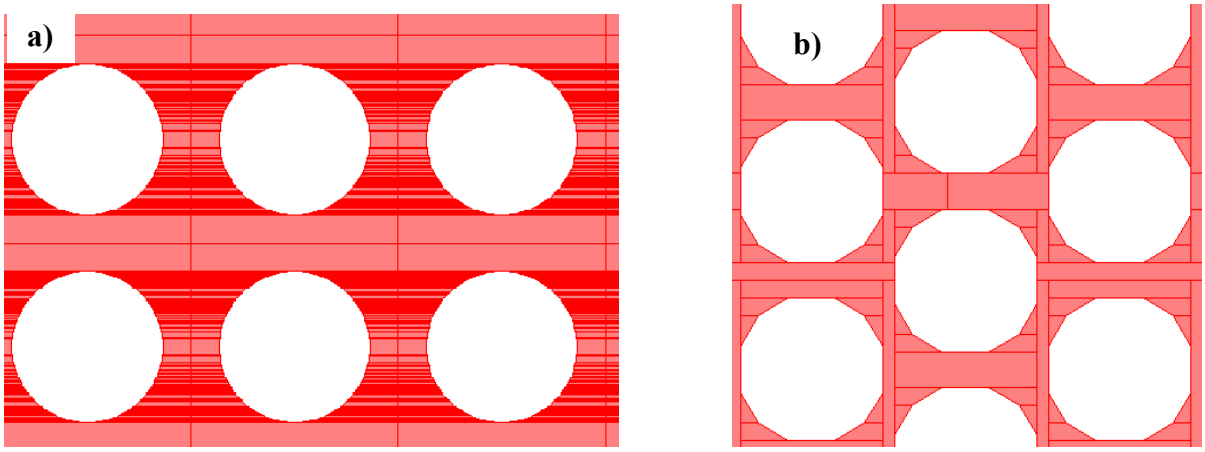



Figure 1. The optimal fracturing of curved layouts is a key data-preparation technology for e-beam direct write and mask production. The fracturing of circular phonic crystals with conventional fracturing (a) and optimized curved fracturing. The conventional fracturing introducing fractures at the vertices produced by the design software is leading to a large number of thin nonuniform sliver increasing the exposure time and resulting poor exposure quality. Curved fracturing is detecting the curved shape (design intent) and introducing optimal fractures for the exposure.

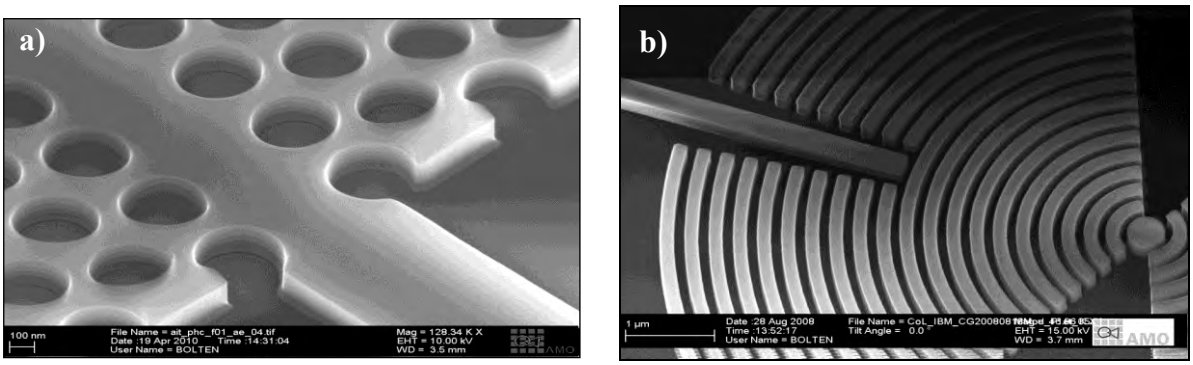



Figure 2: SEM micrograph of a) a photonic crystal based defect waveguide. Design by AIT, fabricated by AMO b) a circular grating resonator with coupling waveguides. Design by IBM Research Zurich, fabricated by AMO.

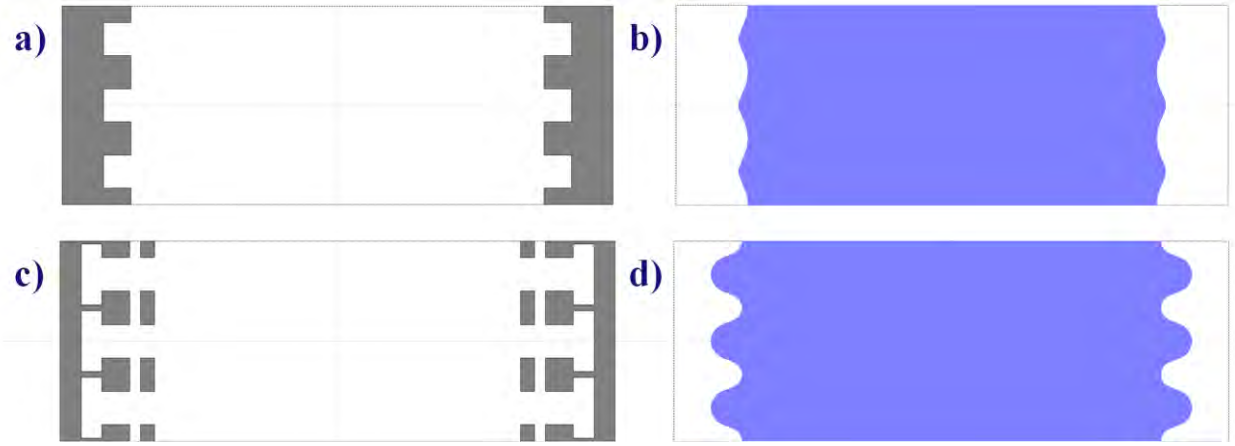



Figure 3: a) Original reticle design at wafer level size by Eindhoven University of Technology with Chrome pattern represented in white, of 1.5 µm waveguide with 240 nm pitch sidewall grating at 200 nm width increase b) Simulated resist profile represented in purple using ArF 193 nm scanner lithography c) Adjusted reticle design with application of hammerhead and scatter bar OPC rules d) Resulting simulated resist profile of OPC adjusted design

# Curvilinear Data Processing Methods and Verification

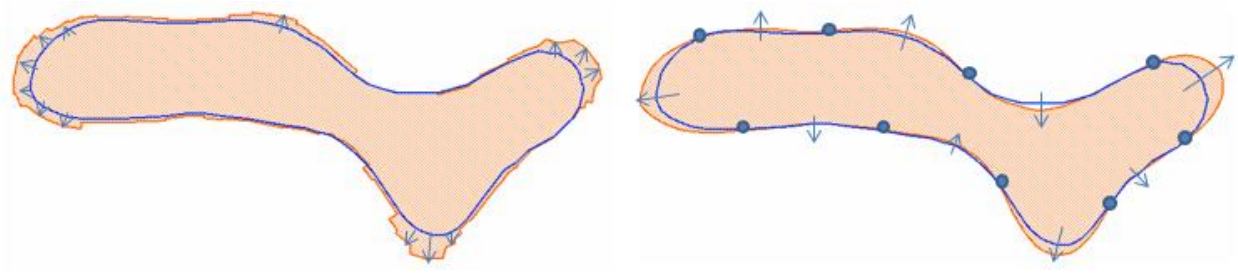
Clyde Browning, Serguei Postnikov, Matthieu Milléquant, Sébastien Bayle, Patrick Schiavone

Aselta Nanographics, 7 Parvis Louis Néel, Grenoble, France

## ABSTRACT

Designs for photonics devices on silicon relies on non-Manhattan features such as curves and a wide variety of angles. Reticle Enhancement Techniques (RET) that are commonly used for CMOS manufacturing now are applied to curvilinear data patterns for the same reasons of enhancing pattern fidelity. Common techniques for curvilinear data processing include Manhattanization, jog removal, and jog alignment. We propose a novel method of describing curvilinear shapes in terms of curves reconstructed by a certain algorithm between control points. Such representation of curvilinear shapes brings many benefits in terms of pattern description (improved fidelity, file compaction), correction and verification. For example it allows smooth displacements during the design correction procedure for proximity effects. The conventional correction by biasing each fragment is shown in Figure1a. Figure 1b illustrates the curve-based biasing where only the control points have been moved and the corrected shape was then reconstructed by connecting the control points in their new positions by the new curves. This method results in faster computation because there are fewer locations to adjust geometry, easier convergence and intrinsic continuity between edges. It also affords significant reduction of the design file size. Another example of application of the new sizing algorithm is presented in Figure 2 in order to enhance the lithographic process margin for a photonic structure like Y-junction. A local biasing was applied and one scatter bar added on each side only where the Y-junction width was smaller than some dimension CD max. In order not to create additional sources of photonic signal attenuation, it is important that the bias value is gradually reduced to zero as the Y-junction width increases with very smooth transitions to the remaining (unbiased) part of the waveguides without jogs or wiggles.

Besides processing curvilinear pattern data, verification is also required after any original pattern modifications. Mask Rule Checks (MRC) are considered as standard step in any design data preparation flows, but the conventional MRC algorithms are conceived for Manhattan designs and as such they often results in numerous false errors or even missing errors when applied to photonics or ILT (Inverse Lithography Technology) designs. In addition, MRC for photonic layouts require much more than basic width and space checking. We developed a verification technology compliant with curvilinear layouts. The new MRC technique is also based on curve representation of the original design comparing directly the curves instead of the straight fragments. It permits to have only one error flag per curve instead of multiple errors seen in fragment-by-fragment MRC, e.g. only three error flags resulted from the new MRC algorithm, see Figure 3. Whereas conventional MRC would yield as many error flags as there are fragments along the highlighted shapes rendering MRC error inspection over the entire design virtually impossible simply due to overwhelming number of error flags. In addition, the API (application programming interface) allows for customization of the MRC that are different from the conventional checks, e.g. corner-to-corner, line-end detection, nubs/notches, angles, circles, curvatures, polygon interactions, design intent integrity.



a) b)

Figure1. Conventional correction by biasing each fragment (a), curve-based biasing where only the control points have been displaced (b).

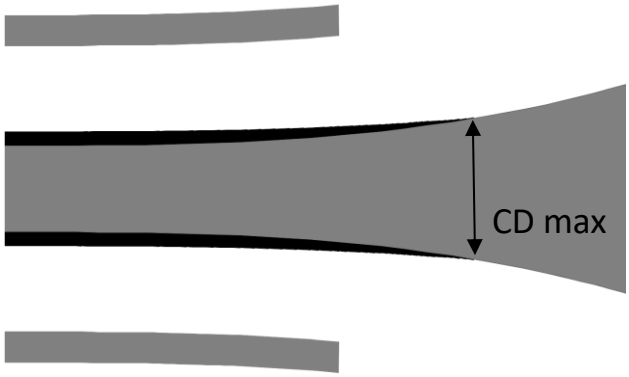



Figure 2. The gradually decreasing bias (solid black contours) starting at Y-junction end and diminishing to 0nm as the waveguide width reaches CD max. One curvilinear scatter (in grey) bar is placed on each side of the Y-junction.

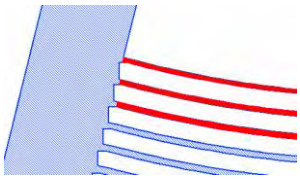


Figure 3. MRC width errors detected in the SPGC device: only three error flags resulted from the curve-based MRC.

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# A Resist Reflow 3D Compact Model Approach for Imager Microlens Applications.

Sébastien Bérard-Bergery*[a], Jérôme Hazart[a], Patrick Quéméré[a], Charlotte Beylier[b], Nacima Allouti[a], Maryline Cordeau[a], Raphaël Eleouet[a], Florian Tomaso[a], Jean-Baptiste Henry[a], Alain Ostrovsky[b], Valérie Rousset[b], Vincent Farys[b]

[a]CEA LETI, MINATEC CAMPUS, 17 rue des Martyrs, Grenoble, France,
[b]STMicroelectronics, 850 Rue Jean Monnet, Crolles, France
*sebastien.berardbergery@cea.fr

## ABSTRACT

In the recent years, there has been a large spreading of optical applications, either embedded into complex multi-function devices such as smartphones, or for imaging purpose as cameras. Core of such optical systems are microlens arrays, widely used for light gathering or light extraction. Many fabrication methods have been developed to manufacture such objects. Among them, probably the most widely used nowadays by the industry is the photoresist thermal reflow method (Figure 1), as proposed by Popovic in 1988 [1].

Coupled with the photolithography technic to produce photoresist patterns, the method consists in melting the photoresist structures in order to form small lens, shaped by the result of the surface tension of the liquid resist. Thus, microlens produced by such means tend to be spherical-like objects. The determination of a microlens size is quite often driven by the size of the pixel that has to be covered. To maximize the device efficiency, the microlens shape is obviously optimized: pixel coverage, height and overall 3D form are key elements.

The final microlens shaping is directly linked to several parameters: the intrinsic photopolymer properties, the initial resist pattern size, and the melt process conditions. The microlens shape optimization is an empiric and iterative task where process variations are explored: resist thickness, lithography exposure conditions, melt temperature and duration. Photomask iterations might be needed to drive in parallel the initial photoresist shape. This '*try-and-retry*' process leads to a costly and time consuming work.

A reflow modeling solution is proposed to solve these issues and make the overall microlens optimization process easier. This method predicts the microlens formation through melt and help creating microlens associated design on the photomask. Some modeling attempts and simulation studies can be found in the literature, exhibiting interesting results - but limited in 2D applications [2,3]. 3D rigorous simulations using physical model might give accurate results too, but their too long computation time is hardly compatible with industrial standards [4].

In this work, we propose a 3D compatible and computation efficient simulation software based on a compact model (Figure 2) calibrated on experimental data. Our software is in line with a Design Process Technology Co-optimization (DTCO) approach. It indeed allows the fast 3D reflow simulations of hundreds of different resist patterns, starting from a CAD design and giving by simulation the corresponding 3D microlens that will be formed. It thus helps lithographers and designers in making the right shape to draw on the layout, leading at the end of the process flow to the expected microlens. The automation flow also increases the reliability and the reproducibility of all the procedure.

We will illustrate a typical use case of the proposed solution, showing how the software efficiently enables lithographers to perform a wide range of design screening. The compact model assessment on experimental data will also be discussed (example in Figure 3).

**Keywords**: Imager, Microlens, Thermal Reflow, 3D Resist Model, Compact Model, Design Process Technology Co-Optimization

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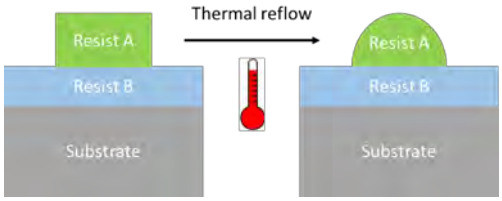


**Figure 1:** Photoresist thermal reflow principle illustration.

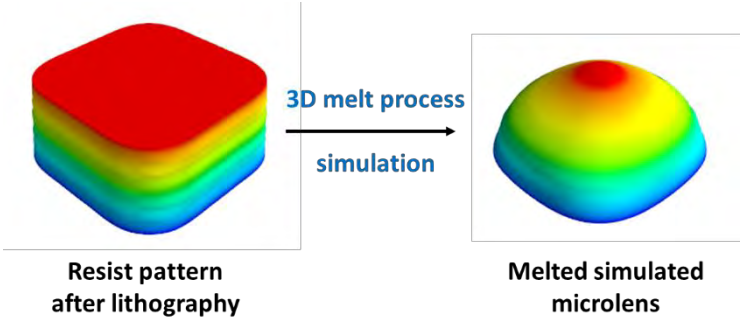


**Figure 2:** Visual illustrations of the compact model software solution rendering while simulating the reflow of rounded square resist pattern.

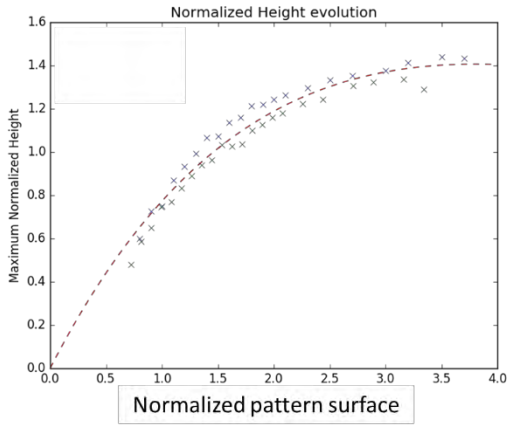


**Figure 3:** Maximum height extracted from 2 types of microlens measured by AFM, compared to the compact model height prediction (dashed red line).

# Tilted beam SEM, a novel approach for industry 3D metrology

C. Valade*[b], J. Hazart[a], S. Bérard Bergery[a], E. Sungauer[b], M. Besacier[c], C. Gourgon[c]
(a): Univ. Grenoble Alpes, CEA-LETI, DTSI, F-38000 Grenoble, France
(b): STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France
(c): Univ. Grenoble Alpes, CNRS, CEA-LETI Minatec, LTM F-38054 Grenoble, France
* charles.valade@cea.fr, charles.valade@st.com

## ABSTRACT

In the microelectronics industry, much of the dimensional metrology relies on Critical Dimension (CD) estimation (the notation convention is given in Fig.1). These measurements are mainly performed by Critical Dimension Scanning Electron Microscopy (CD-SEM), because it's a very fast and mainly non-destructive method, in addition these type of SEM are able to make measurements directly on wafers.
To measure the CD, we estimate the distance between the edges of the observed pattern on a SEM image. As the critical dimension becomes smaller and smaller, the needs for more reliable metrology technique emerge.

In order to obtain more meaningfull and reproductible CD measurements regardless of the pattern type (line, space, contact, hole …), one needs to perform a CD measurement at a known and constant height thanks to a methodology that determines the topographic shape of the pattern from SEM images.
Using a SEM capable of bending the electron beam (up to 12° in our case), two images of the pattern are taken from two different angles (Fig2). From them, pattern height and sidewall angle can be consequently determined using geometries considerations detailed in Fig3.

From these images, we determine quantities related to the characteristics of the pattern that we then correct using a model, in order to get measurements that are not too much affected by eletronic artefact, characteristic of SEM images, especially in tilted mode. This model is calibrated thanks to reference measurements made with an AFM or a FIB SEM/TEM.

Since there is an electronic interaction between the pattern shape/material and the electrons of the beam resulting in the image formation, it is important to understand the electronic response of the SEM according to the pattern topographies, the beam conditions, the material, the stack ...
To better understand the electronic effects encountered, a preliminary work based on Monte-Carlo simulation is conducted using the JMONSEL software. This analysis is conducted in order to anticipate trends on the measurements for different topographies and tilt beam conditions.
The Fig.4 show the impact of the corner rounding (CR) on SEM images taken in topview. From this analysis we can observe that the presence of a CR at the bottom of the edge does not influence the electronic response of the top of the pattern and vice versa with the top CR.
It has also been possible to find a "first approximation" correction function allowing to recover the value of the CR top and bottom from the quantities found thanks to the SEM images.

The purpose of this presentation is to show some of the simulations results, and explain the general approach that will be used in order to create a model able to recover topographic informations from different tilt SEM images.

Keyword: SEM, CD, metrology, sidewall angle, height, edge width, topography, model, JMONSEL

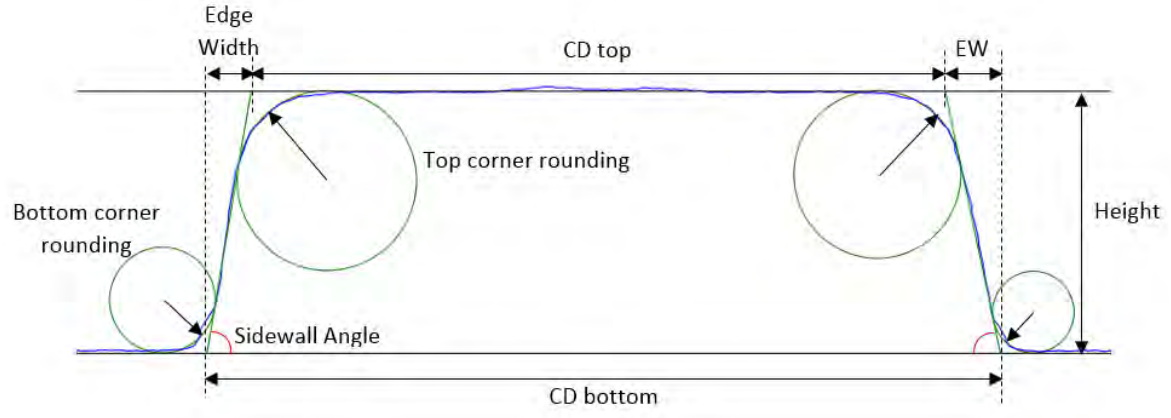


*Fig.1: Sectional view of a "line" type pattern (in blue) with all the notations used to characterize it*

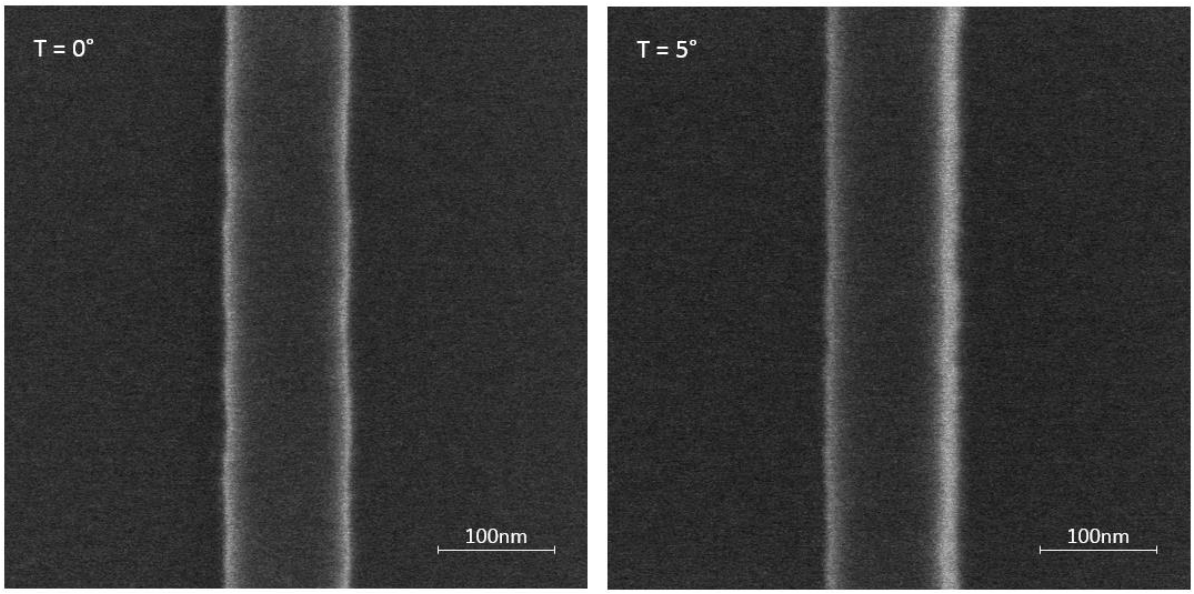


*Fig.2:* *Images taken with a tilted beam CD-SEM (Verity4i from AMAT) in topview and with a 5° tilt angle. Pattern: Etch silicon, h = 100nm, CD = 100nm*

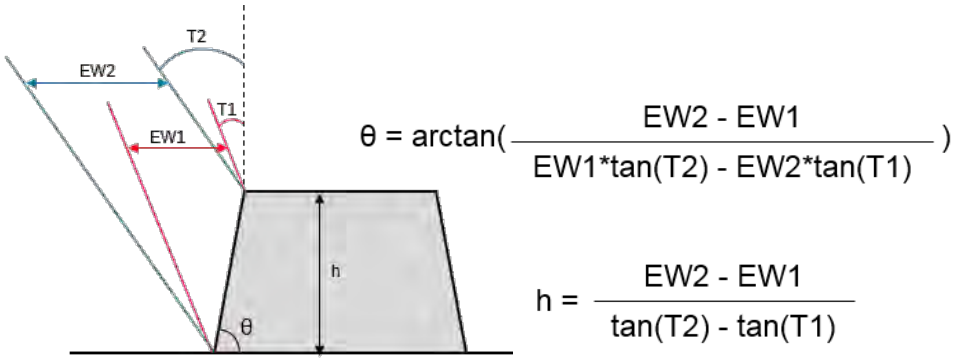


*Fig.3:* *Geometric resolution of the height and sidewall angle of a pattern, thanks to two images taken at two different tilt T1 and T2 leading to two different edge width EW1 and EW2.*
*From :* *Addressing FinFET metrology challenges in 1X node using tilt-beam CD-SEM, Xiaoxiao & al, SPIE 2014*

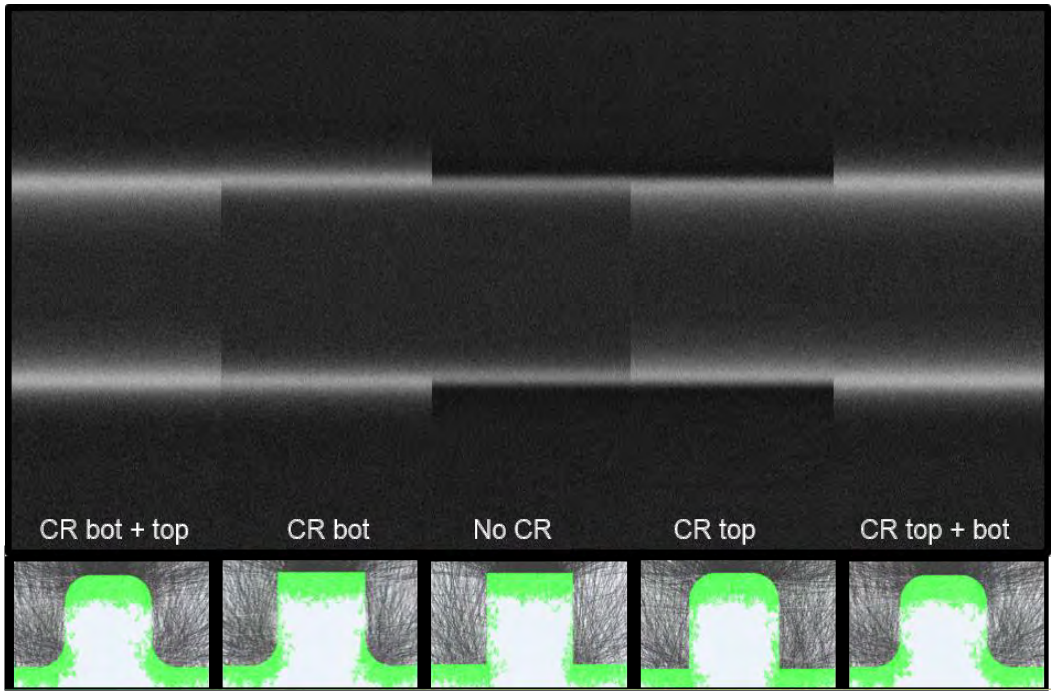


*Fig.4:* *Example of a processed result from JMONSEL: Effect of the corner rounding top and bottom on a SEM image in topview.*
*Pattern: Etch silicon, h = 100nm, CD = 100nm, swa = 90°, CR = 0 or 30 nm*
*Beam cond: Vacc = 800V, pixel size = 0.5*0.5 nm, Electrons/pixel = 10k, spot size = 2nm*

# On the Road to Automated Production Workflows in the Back End of Line

Gilles Tabbone, Kokila Egodage, Kristian Schulz, Anthony Garetto

Carl Zeiss SMT, Carl-Zeiss-Promenade 10, 07745 Jena, Germany

## Abstract

The technical roadmap adopted by the semiconductor industry drives mask shops to embrace advanced solutions to overcome challenges inherent to smaller technology nodes while increasing reliability and turnaround time. It is observed that the turnaround time is increasing at a rapid rate for each new ground rule[1]. At the same time, productivity and quality have to be ensured to deliver the perfect mask to the customer. These challenges require optimization of overall manufacturing flows and individual steps, which can be addressed and improved via smart automation.

Ideally, remote monitoring, controlling and adjusting key aspects of the production would improve labor efficiency and enhance productivity. It would require collecting and analyzing all available process data to facilitate or even automate decision-making steps. In mask shops, numerous areas of the back end of line workflow have room for improvement in regards to defect disposition, reducing human errors, standardizing recipe generation, data analysis and accessibility to useful and centralized information to support certain approaches such as repair. Adapting these aspects allows mask manufacturers to control and even predict the turnaround time that would lead to an optimized process of record.

A cost-productivity model[2] has been previously established to quantify the overall turnaround time of masks along with the probability of errors arising during the manufacturing process. Such a model allows identifying process segments that have the potential for automation and would benefit in terms of increased productivity. In this paper, a full repair workflow is performed using a programmed defect mask (PDM) in order to demonstrate the extent of software based automated solutions. The tools utilized for the procedure are standard repair and review tools such as MeRiT® and AIMS™. Software applications under the FAVOR® brand, such as the aerial image evaluation software, AIMS™ AutoAnalysis (AAA), and the SEM image evaluation software, SEM AutoAnalysis (SAA), are adapted to support the different steps of the mask production workflow. These applications conduct image evaluation in parallel to image capture that enables turnaround time reduction. Tool activity, applications, masks and defects are tracked throughout the repair process by the overarching manufacturing enterprise solution, Advanced Repair Center (ARC) that centralizes all process data and enables quick decision-making. The sequence implemented is a possible illustration among others but describes a realistic workflow.

The starting point of the sequence is a mask inspection report that issues points of interest on the mask. A MeRiT system takes SEM images of all locations, as well as reference images, which would normally trigger a SEM image analysis via SEM AutoAnalysis. However, in this attempt the software is used as a stand-alone. The user is notified if the points of interest are defective or not. While keeping the mask inside the MeRiT tool the newly confirmed defects will be repaired. The mask is then

[1] The Mask Maker Survey 2017, eBeam Initiative

[2] K. Schulz, K. Egodage, G. Tabbone, A. Garetto, "Improving back end of line productivity through smart automation", Proc. SPIE 10451, Photomask Technology

transferred to an AIMS system that images the repaired defects followed by a thorough analysis performed by AIMS AutoAnalysis. This produces a detailed report of the repair quality and qualifies the defects with respect to specifications. In the meantime, all the processes and results are tracked by the Advanced Repair Center, which automatically records the activity of the mask, tools as well as the measurement data and enables quick decision-making (Figure 1).

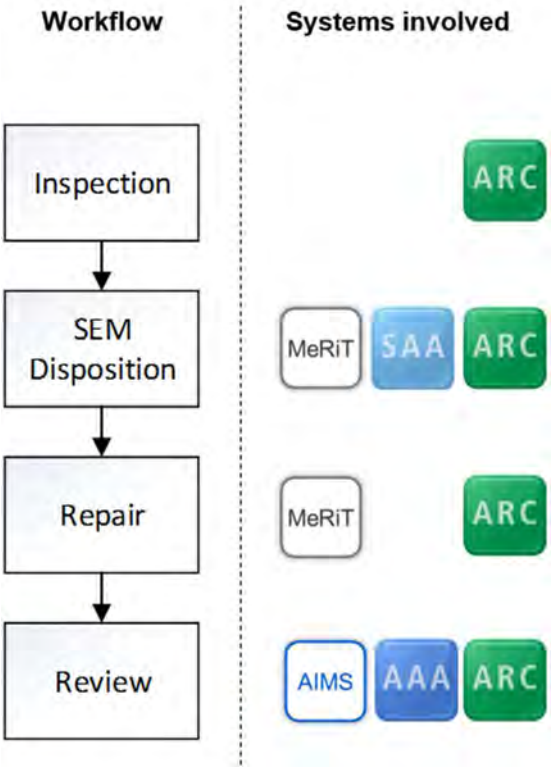


*Figure 1: Proposed workflow vs. systems*

This example illustrates the implementation of intelligent automation in the back end of line and highlights the benefits mask makers could harness.

**KEYWORDS:** AIMS, MeRiT, review, repair, SEM, automation, FAVOR, BEOL

# Measuring inter-layer edge placement error with SEM contours

François Weisbuch[a], Jirka Schatz[a]
[a]GLOBALFOUNDRIES Dresden, Wilschdorfer Landstrasse 101, D-01109 Dresden

## 1. BACKGROUND

For advanced technology nodes, the patterning of integrated circuits requires not only a very good control of critical dimensions (CD) but also a very accurate control of the alignment between layers. These 2 factors combine to define the metric of edge placement error (EPE) [1,2,3] that quantifies the quality of the pattern placements critical for yield. Usually, EPE (design) refers to the deviation of an edge placement with respect to the design intent. A better definition to take into account the influence of the overlay between layers, is to consider the EPE (inter-layer) that can be defined as the relative distance between the edge of a pattern on layer A to the edge of a second pattern on layer B (see Fig1,2). This metric quantifies the process margin in term of min distance between a pattern of layer A to a pattern of layer B (for example, it can capture potential electrical shorts). It can also be used to assess the overlap between a pattern of layer A and a pattern of layer B (for example for calculating contact resistance or identify open issues).

In this work, we consider the edge placement errors between a contact layer (CA) with respect to poly layer (PC) as illustrated in Fig. 1. Precise inter-layer overlay measurement between complex features cannot be achieved accurately with traditional alignment marks because of the limited amount of alignment marks intra-field and specific local litho/etch response. With traditional CD SEM measurement, it is very challenging to derive intra layer measurement or area of overlap.

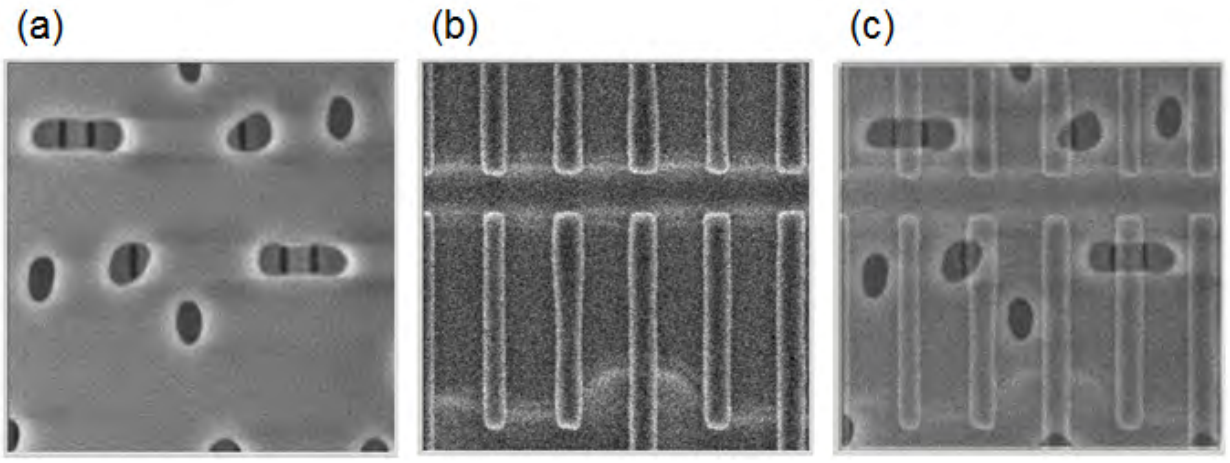


**Fig.1**: *Illustration of intra-layer edge placement error. (a) SEM picture of contact layer after etch. (b) SEM picture of poly layer after etch. (c) Blending both pictures to illustrate the challenge of controlling and measuring contact to poly edge placement error.*

The goal of this work is to present a method based on SEM contours to get a robust and direct measurement of inter-layer edge placement errors and between patterns overlap area. The motivation is also to assess the variation of these measurements across wafer for various critical patterns. In particular, one objective is to identify the contribution of CD and overlay errors in the total EPE budget.

## 2. APPROACH

To derive the edge placement error between CA and PC patterns, SEM pictures were acquired sequentially at the final etch operation of each layer. Around 10 critical patterns of both layers were measured across wafer (around 100 fields) at exactly the same locations. Contours extracted from SEM pictures were post-processed to remove flyers. CA contours need to be finely aligned with PC contours. This is done for each fiel/ pattern combination by aligning the SEM pictures of CA relative to PC.

From all SEM contours (see Fig.2), it is possible to measure the PC to CA overlap, the CA to PC distance and the PC to CA misalignment and compare with standard overlay measurement. In addition, combining the contours allows estimating the CD variability across wafer for each individual pattern.

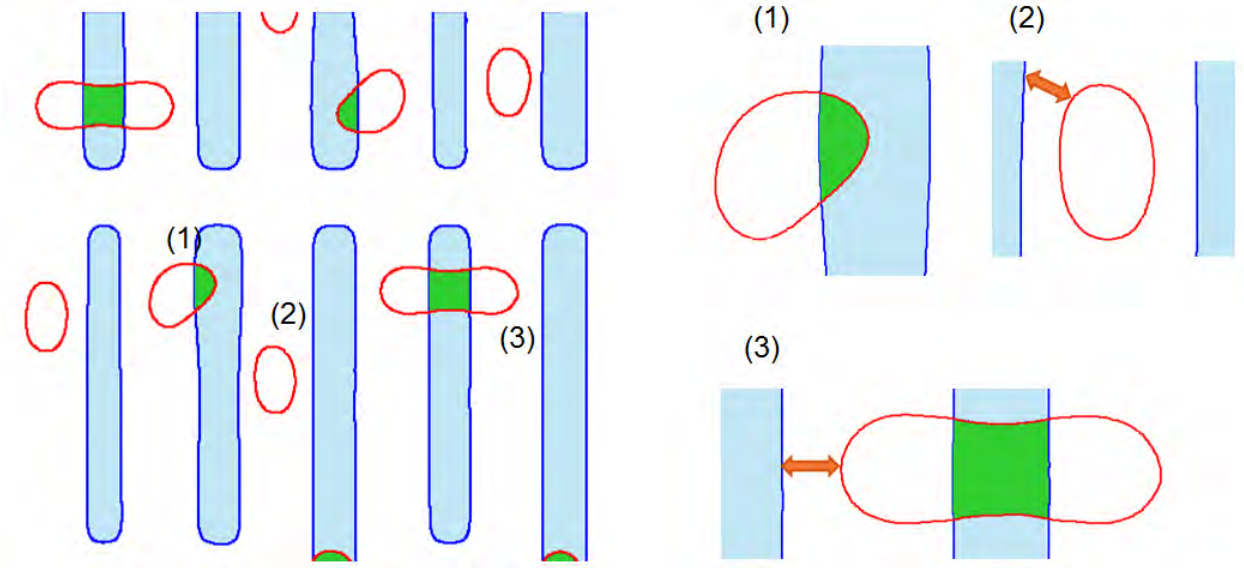


**Fig. 2:** *Overlap of SEM contours of PC (blue) and CA(red) extracted after etch. The analysis of the contours allows measuring (1) CA to PC overlap, (2,3) CA to PC distance*

[1] Jan Mulken et al., "Patterning control strategies for minimum edge placement error in logic devices," Proc. SPIE 10145, Metrology, Inspection, and Process Control for Microlithography XXXI, 1014505 (28 March 2017)

[2] Jacek K. Tyminski, Julia A. Sakamoto, Shane R. Palmer, Stephen P. Renwick, "Lithographic imaging-driven pattern edge placement errors at the 10-nm node," J. Micro/Nanolith. MEMS MOEMS 15(2) 021402 (30 March 2016)

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# FEM Simulation Of Charging Effect During SEM Methodology

Duy Duc Nguyen[1,2], Jean-Herve Tortai[2], Mohamed Abaidi[1], Patrick Schiavone[1]

**Emails**: *duy-duc.nguyen@aselta.com, jean-herve.tortai@ltmlab.fr, patrick.schiavone@aselta.com, mohamed.abaidi@aselta.com*

[1]ASELTA Nanographics, MINATEC - BHT 7, Parvis Louis Néel 38040 Grenoble cedex 9 - France

[2]Laboratoire des Technologies de la Microélectronique (LTM), CNRS/UJF CEA / LETI / Minatec 17, avenue des Martyrs 38054 Grenoble cedex 9 - France

**Abstract**

The SEM image is an image of the sample surfaces observed by Scanning Electron Microscope (SEM). The specimen is placed under an electron gun which shots an electron beam to the specimen causing secondary electrons to emit from the specimen surface. These electrons are collected by secondary electron detector and that produces a signal which is transferred to the display unit as a greyscale pixel, Figure 1 [1].

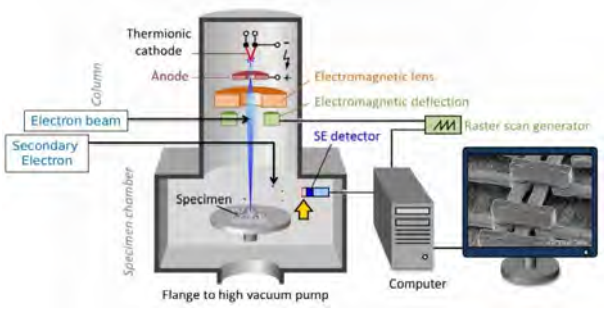


Figure 1: Sketch of how SEM image is created.

Influence of charging on SEM image happens when the specimen has an excess or a lack of electrons, [1]. Precisely, there are two kinds of charges; negative charge occurs when electrons are entrapped in the specimen while positive charge excess appears when the number of the electrons exiting from the specimen is larger than that flowing to the specimen. Charging effect is caused by the fact that secondary electron trajectory is influenced by negative or positive charges excess. If the specimen is negatively charged more secondary electrons enter the detector, so that the locally charged area is observed bright. Whereas, if the specimen is positive charged, less secondary electrons enter the detector, so that the locally charged area is observed dark. For example, Figure 2 [2] shows an affected SEM image with negative charging leading to unnormal bright area followed by a black tail and an un-affected SEM image for comparison.

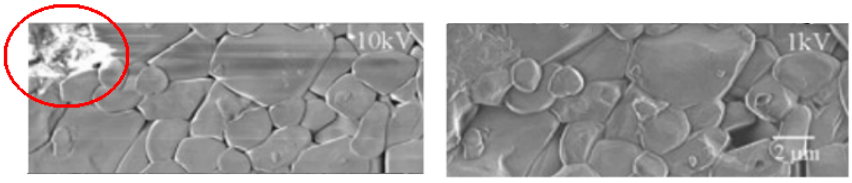


Figure 2: Affected SEM image with anomalous tailing comparing to un-affected one.

Charging can significantly impact CD-SEM metrology. In order to remove this influence, we have to understand how the charges and the potential behave under the incident electron beam on the sample with

[1]The picture is taken from published lecture of Karlsruhe University of Applied Sciences, Germany.
[2]The picture is taken from [1].

various surface topologies and materials. The classical drift-diffusion model is a good candidate because it shows fundamental semiconductor physics such as the motion, generation and recombination of charges in relation with the electrical field. The drift-diffusion model is a system of Partial Differential Equations (PDEs) with of the diffusion and drift equations. The diffusion equation points out the net movement of charges from a region of high concentration to a region of low concentration and it is described mathematically as the divergence of gradient of the charges. The drift equation shows the transport of charges within electric field and it is described mathematically as the divergence of the charges multiplied with velocity field and is similar to the fluid's motion. Moreover, to represent the dynamic evolution of charges over time, their rate of change are added into the drift-diffusion equations. As charges are generated, the potential changes and diffuses. In turn, the electric field created by the potential affects the flow of the charges. Solving such PDEs system necessitates postulating for initial conditions and boundary conditions. We assume that there is no charges at the edges of the sample and at the beginning of time.

$$\begin{cases} \varepsilon_0 \varepsilon \nabla \cdot \boldsymbol{E} = q_e \left(p - n\right) & \text{in} \quad \Omega \times (0, t_{end}] \\ \dfrac{\partial n}{\partial t} = \dfrac{1}{q_e} \nabla \cdot \boldsymbol{J}_n + S - R & \text{in} \quad \Omega \times (0, t_{end}] \\ \dfrac{\partial p}{\partial t} = -\dfrac{1}{q_e} \nabla \cdot \boldsymbol{J}_p - R & \text{in} \quad \Omega \times (0, t_{end}] \end{cases} \tag{1}$$

$$\text{with } \boldsymbol{J}_n = q_e \left(\mu_n n \boldsymbol{E} + D_n \nabla n\right), \ \boldsymbol{J}_p = q_e \left(\mu_p p \boldsymbol{E} - D_p \nabla p\right),$$

$$\text{and } \varphi = p = n = 0 \text{ on } \Gamma_0, \nabla\varphi \cdot \boldsymbol{\eta} = \nabla p \cdot \boldsymbol{\eta} = \nabla n \cdot \boldsymbol{\eta} = 0 \text{ on } \Gamma_N \text{ and } \varphi, p, n(t=0) = 0,$$

where $\Omega$ denotes a given scanned surface or volume, Figure 3, $\partial\Omega$ denotes the boundary of $\Omega$, $\Gamma_0$ and $\Gamma_N$ denotes portions of $\partial\Omega$ where Dirichlet and Neumann boundary conditions are applied, each point in $\Omega$ is denoted by $\boldsymbol{x} = (x_i)$, $i \in \{1, 2\}$ or $i \in \{1, 2, 3\}$, $t \in (0, t_{end}]$ denotes time variable and time interval, $p\left(\boldsymbol{x}, t\right)$ and $n\left(\boldsymbol{x}, t\right)$ denote hole and electron densities, $D_n$ and $D_p$ denote electron and hole diffusion coefficients, $\mu_n$ and $\mu_p$ denote electron and hole drift mobilities, $\boldsymbol{J}_n\left(\boldsymbol{x}, t\right)$ and $\boldsymbol{J}_p\left(\boldsymbol{x}, t\right)$ denote electron and hole currents respectively. The notation $\boldsymbol{E} = -\nabla\varphi$ denotes electric field with $\varphi\left(\boldsymbol{x}, t\right)$ is potential, $\varepsilon_0$denotes absolute permittivity of the vacuum, $\varepsilon$ denotes relative permittivity and $q_e$ denotes elementary charge. The notation $S\left(\boldsymbol{x}, t\right)$ is the source term which is expressed in a Point Spred Function (PSF) form. Once electrons are entrapped in the sample, a rapid recombination term appears that tends to compensate for this electron excess so electro-neutrality is maintained shortly. In our implementation, this recombination term, denoted $R\left(\boldsymbol{x}, t\right)$ follows Shockley-Read-Hall model [2][3][4][5] formulated by

$$R(n,p) = \frac{np - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)}, n_1 = N_c exp\left(\frac{E_t - E_c}{kT}\right), p_1 = N_v exp\left(\frac{E_v - E_t}{kT}\right) \tag{2}$$

where $n_i$ denotes intrinsic carrier concentration, $\tau_n$ and $\tau_p$ denote electron and hole average lifetime, $N_v$ and $N_c$ denote effective density of states according to valence and conductor bands, $k$ denotes Boltzmann constant and $T$ denotes temperature.

The analytical solution of the PDEs (1) generally can not be found for the vast majority of geometries. Instead, an approximation of the PDEs (1) is constructed by discretization methods, for instance, the Finite Element Method (FEM) is our choice. We have chosen FEniCS to be our simulation tool. FEniCS is a well-known open-source computing platform for quickly translating scientific models into efficient finite element code. To start the numerical method process, the PDEs (1) is transferred into a simplified form called weak formulation that enables using the concepts of linear algebra to solve the problem. In addition, Finite Elements necessitates a mesh that will define elementary sub-domains. Computation time is strongly related to the number of sub domains, the best compromise being adaptive mesh were resolution is increased where it is needed while large mesh can be used where smooth parameter variation occurs. In our case, the adaptive mesh is created by an open software called GMSH Figure 3. Using adaptive mesh reduces the computation time enormously (factor 15-20). Typically, the fine mesh is set only in the neighbourhood of the excitation beam instead of everywhere in the domain.

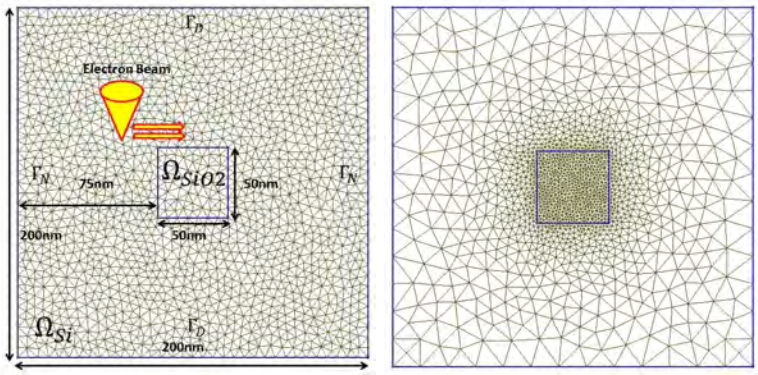


Figure 3: Plot of geometry of $\Omega$ used in top-view simulation showing the starting point of the electron beam and its direction; the uniform and adaptive meshes built by GMSH; the adaptive mesh has the scanning area refined up to $1[nm]$.

In order to be able to generate an image-like simulation, we implemented the scanning mode of solution. The incident beam $S$ goes from the left to the right and from the top to the bottom of the specimen surface. Besides, it stays $t_{spot} = 50\,[ns]$ at each pixel of $4\,\left[nm^2\right]$. In two dimensional space, we introduce top and slice-view simulations which allow us to observe the distribution of the electron and the potential in x-y directions or in z-direction. In three dimensional space, we introduce simulations similar to ones in two dimensional space. In the examples given in the presentation, the specimen is made of Silicon (Si) and the pattern is made of Silicon dioxide (SiO2), for example see Figure 4. This figure illustrates a few results of computation of the charge and potential repartition at different steps of the scan mode. It shows that the electron concentration are much higher in SiO2 pattern than Si base which indicates that the charging effect should occur mainly in the SiO2 pattern.

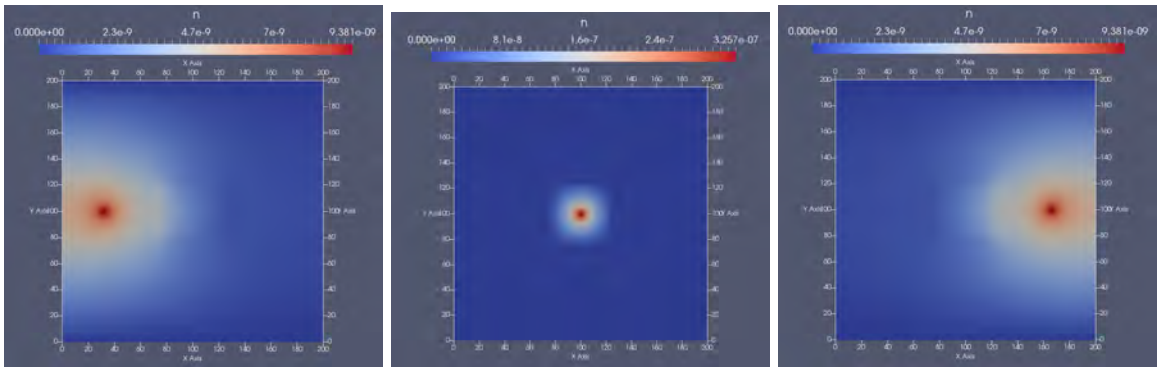

Figure 4: Plot of geometry of $200 \times 200\,\left[nm^2\right]$ Silicon blanket with one $50 \times 50\,\left[nm^2\right]$ SiO2 pattern; the concentration of electron increases properly when the electron beam irradiates the pattern.

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# Automatic Defect Classification of SEM images using Deep Learning

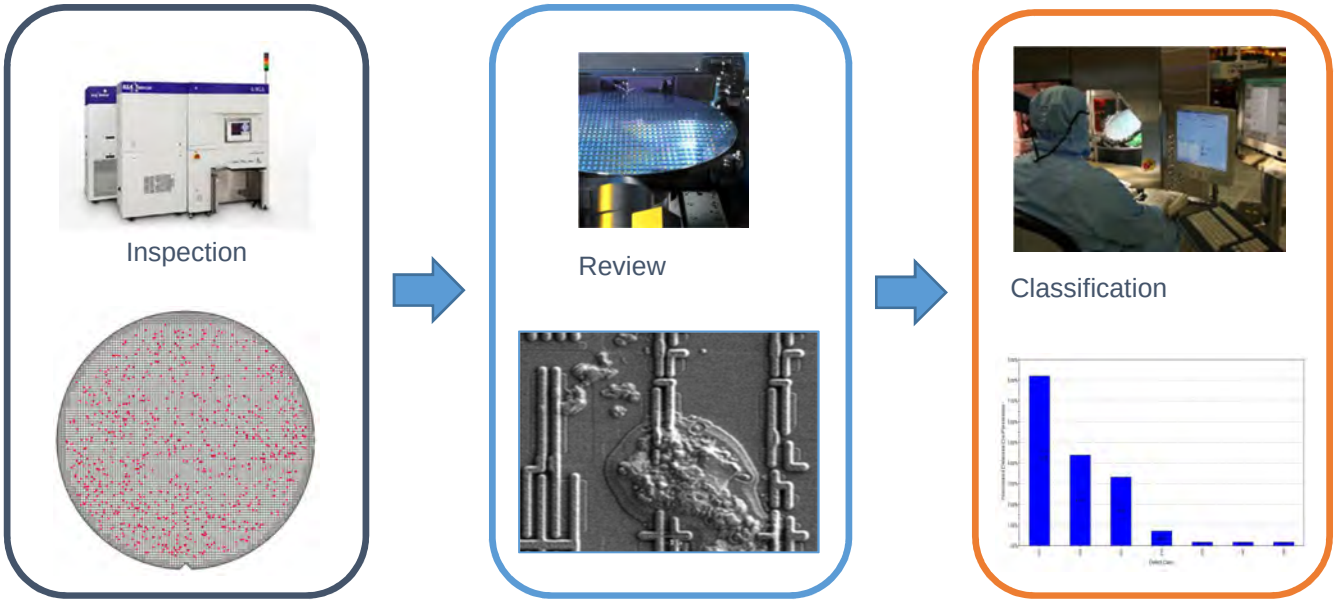
Laurent Bidault (STMicroelectronics Rousset, France)
Dario Mastroeni (STMicroelectronics Rousset, France)

## 1. Overview of the project

All along the production line, physical defects are sometimes generated by the process equipments.

To control the quality of our chips, we need to inspect the wafers periodically to know more about these defects.

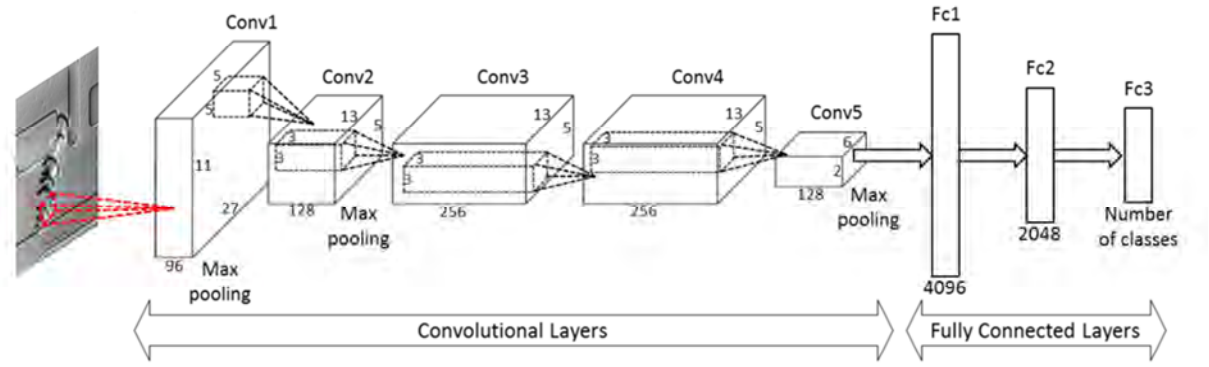
One important task is to take **images** of these defects by an Electronic Microscope (SEM). Once we have those images, operators have to “manually” classify them according to the family they belong to.




This task is difficult, time-consuming and prone to human sensitivity.

To work around these issues, we have developed and integrated an algorithm based on modern **Convolution Neural Network** architecture (**Deep Learning**) which is able to recognize the content of the pictures and to classify them.

## 2. Results




How a Deep Neural Network Works

The algorithm is running **in production** for more than **18 months** with **100% uptime** and makes up to **2 times less errors than well-trained operators (around 95% accuracy)**.

There are already **20 inspection layers on production** with a number of **classes** between **7 and 13** for each one.

In each layer, **all the products** are represented.
Sometimes (mainly on the Back end) **it is possible to group several layers** on the same configuration which is a huge gain of time during dataset creation used for training the algorithm.

It is to notice also that this algorithm is able to “refuse” the classification if the prediction is unsure. This specific behavior is done only for a small number of images so that the contribution rate **(% of classified images**) is around **93%** (only 7% of images unclassified).
By this way, we are able to **detect “novel class”** when it happens.

One important feature of this algorithm is that **it just needs one image per defect**: there is no need to collect a reference image (image with no defect) on the neighboring ship.

The result is a **“real-time” classification** (1 second per image) which is absolutely essential to follow the need of the production.

# Deep Supervised Learning to Estimate True Rough Line Images From SEM Images

N. Chaudhary, S. A. Savari[1], S. S. Yeddulapalli
*Texas A&M University, College Station, TX 77843-3128, USA*
*savari@ece.tamu.edu*

Line edge roughness (LER) and other stochastic effects in the semiconductor lithographic process will impact the limits of lithographic scaling.[2] For example, extreme ultraviolet lithography increases stochastic fluctuations at a given dose over conventional photolithography because of the reduction in the number of photons.[2] The estimation of LER and other roughness characteristics from scanning electron microscope (SEM) images is therefore of great importance in metrology for the semiconductor industry. Low-dose SEM images are interesting because they reduce resist shrinkage and acquisition time, but they are corrupted by Poisson noise, edge effects, Gaussian blur and other instrument errors. The estimation of line edge geometry and roughness requires techniques to account for these artifacts. Earlier approaches to edge estimation relied on traditional approaches to signal/image processing[3] or on physical model-based regression methods.[4,5] For instance, one common image processing scheme applies a Gaussian denoiser followed by an edge detector with a filter. This approach is known to potentially destroy the fine details of the line edges. The competing physical model-based regression methods are constrained by the accuracy of the modeling assumptions. Our approach is different. We believe that in the presence of enough realistic simulated data supervised machine learning offers the prospect of high-accuracy estimates of the input from the outcome of complex physical processes without the constraints of modeling assumptions.

Deep convolutional neural networks[6] can solve natural image classification problems[7] and achieve superhuman performance on games[8] because they are effective at learning complex nonlinear models. For natural images corrupted by Gaussian noise the state-of-the-art in image denoising is attained by neural networks.[9,10] Since semiconductor metrology has important inverse problems, deep supervised learning has the potential to advance the discipline.

In this paper, we propose the use of deep supervised learning for the denoising of SEM images; we concentrate here on Poisson noise and rough line images, but if there is sufficient realistic simulated data the approach can be extended to the study of other detection and estimation problems such as the estimation of rough contours and the detection of microbridges and missing contact holes. We argue that this approach to SEM denoising preserves the fine details of edges and results in better estimates of LER and other roughness characteristics. The training of deep convolutional neural networks requires large datasets. There are currently no publicly available datasets of rough line SEM images, and we plan to offer such a database to facilitate the future development of algorithms.

To create a dataset we used the Thorsos method to generate 20160 random rough

1. Portions of this research were conducted with the advanced computing resources provided by Texas A&M High Performance Research Computing.

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edges each of which follow a Gaussian distribution with an underlying Palasantzas spectral model. Each simulated edge has length 2.048 microns and corresponds to 1024 pixels. To consider a diverse collection of models we generated edges for eight values of LER ($\sigma$ = 0.4, 0.6, 0.8, 1.0, 1.2, 1.4, 1.6, 1.8 nm), nine values of Hurst/roughness exponent ($\alpha$ = 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9) and 35 values of correlation length ($\xi$ = 6, ..., 40). For each of the 2520 possible combinations of parameters $(\sigma,\ \alpha,\ \xi)$ we generated eight edges.

We next used the SEM simulator ARTIMAGEN[11,12] to generate 10080 images of dimension $1024 \times 64$ pixels with pixel size 2 nm $\times$ 0.5 nm; we selected these dimensions to handle the computational demands associated with the training of a deep neural network. Each image contains a line of width 10 nm or 15 nm with two of the previously generated rough edges; the locations of the lines within the images vary. The features of the ARTIMAGEN simulator enabled us to construct images which incorporate random backgrounds, a fixed edge effect, fine structure and Gaussian blur. Our original image set is the collection of these 10080 images. From each original image we generated ten noisy images corrupted by Poisson noise with electron density per pixel in the range $\{2,\ 3,\ 4,\ 5,\ 10,\ 20,\ 30,\ 50,\ 100,\ 200\}$. Thus, the noisy image dataset consists of 100800 images. From the noisy and original images we construct a supervised learning dataset of pairs of images $(x^i,\ y^i)$, where the input $x^i$ is a noisy image and the output $y^i$ is the corresponding original image.

We devised a deep neural network named SEMNet to estimate original images from noisy images with arbitrary levels of Poisson noise. SEMNet consists of 17 convolutional layers, 16 batch normalization layers[13] and 16 dropout layers[14] for regularization. We trained SEMNet on 89280 noisy-original image pairs for four epochs. The training time with a Tesla K80 GPU and Intel Xeon E5-2680 v4 2.40GHz node was approximately 41 hours.

The top left image in Figure 1 shows a noisy test image not used in the training of SEMNet with a noise level of 2 electrons per pixel. The remaining images in Figure 1 consist of the corresponding original image and the images obtained by applying the denoisers of SEMNet, the total variation algorithm (split Bregman optimization),[15] DnCNN[9] and a denoiser based on a Daubechies wavelet.[16] Observe that the quality of the SEMNet denoiser is good even in the high noise regime. Table 1 quantifies the relative performances of the denoisers for three test images in terms of peak signal-to-noise ratio (PSNR) and demonstrates the superiority of SEMNet in different settings. The average denoising time per image of SEMNet was 1.96 seconds on a central processing unit and 0.12 second on the K-80 GPU. This runtime data does not include the time to load the model as this operation was performed only once. We next investigated how to combine the Canny edge detection algorithm with the original and various denoised images from the noisy test images to estimate LER and to compare these values to the true LER of the corresponding edges. Table 1 includes the results for the central 1000 (out of 1024) pixels. The $\sigma_C$ parameters for the Canny edge detection algorithm were chosen to minimize the LER estimation errors. SEMNet again attains the best performance and produces an output which is close to the true edge geometry. The bulk of the results were obtained using the python programming language and the Keras, Tensorflow and scikit-image libraries. The DnCNN image was generated through Matlab's Neural Network toolbox.

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Figure 1. (a) Noisy image with a noise level of 2 electrons per pixel. (b) Estimated image from the deep neural network SEMNet. (c) Corresponding original image without Poisson noise. (d) Total variation (Bregmann method) denoising. (e) DnCNN[9] denoising. (f) Wavelet (db2) denoising.

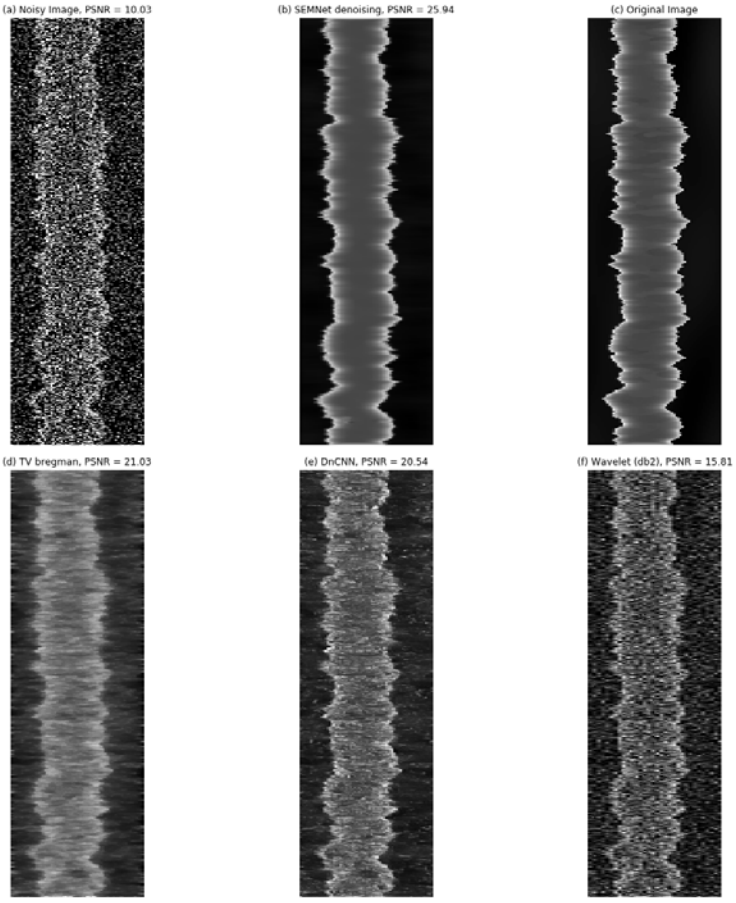


TABLE 1. DENOISING AND LER RESULTS. THE LER DATA IS FOR THE CENTRAL 1000 OUT OF 1024 PIXELS FOR EACH IMAGE.

| Original Image $\sigma$(nm), $\xi$(nm), $\alpha$ | Poisson noise level | PSNR noisy (dB) | Denoiser method | PSNR denoised (dB) | Canny detector $\sigma_C$ | Left edge $\sigma$(nm) (true) | Left edge $\sigma$(nm) (observed) | Right edge $\sigma$(nm) (true) | Right edge $\sigma$(nm) (observed) |
|---|---|---|---|---|---|---|---|---|---|
| 0.8, 10, 0.3 | None | - | None | - | 0.5 | 0.74 | 0.74 | 0.74 | 0.71 |
| 0.8, 10, 0.3 | 10 | 16.22 | SEMNet | 28.63 | 0.5 | 0.74 | 0.68 | 0.74 | 0.69 |
| 0.8, 10, 0.3 | 10 | 16.22 | TV | 22.41 | 1.5 | 0.74 | 0.68 | 0.74 | 0.59 |
| 0.8, 10, 0.3 | 10 | 16.22 | DnCNN | 25.08 | 1.5 | 0.74 | 0.60 | 0.74 | 0.66 |
| 0.8, 10, 0.3 | 10 | 16.22 | Wavelet | 20.86 | 2.5 | 0.74 | 0.64 | 0.74 | 0.58 |
| 1.2, 40, 0.7 | None | - | None | - | 0.5 | 1.07 | 1.07 | 1.21 | 1.20 |
| 1.2, 40, 0.7 | 2 | 10.03 | SEMNet | 25.94 | 0.5 | 1.07 | 1.04 | 1.21 | 1.18 |
| 1.2, 40, 0.7 | 2 | 10.03 | TV | 21.03 | 3 | 1.07 | 1.22 | 1.21 | 1.15 |
| 1.2, 40, 0.7 | 2 | 10.03 | DnCNN | 20.54 | 3 | 1.07 | 1.23 | 1.21 | 1.24 |
| 1.2, 40, 0.7 | 2 | 10.03 | Wavelet | 15.81 | 3 | 1.07 | 1.26 | 1.21 | 1.27 |
| 1.6, 30, 0.5 | None | - | None | - | 0.5 | 1.57 | 1.54 | 1.59 | 1.56 |
| 1.6, 30, 0.5 | 100 | 26.06 | SEMNet | 40.64 | 0.5 | 1.57 | 1.53 | 1.59 | 1.57 |
| 1.6, 30, 0.5 | 100 | 26.06 | TV | 22.59 | 1.0 | 1.57 | 1.53 | 1.59 | 1.55 |
| 1.6, 30, 0.5 | 100 | 26.06 | DnCNN | 30.72 | 0.5 | 1.57 | 1.53 | 1.59 | 1.55 |
| 1.6, 30, 0.5 | 100 | 26.06 | Wavelet | 28.71 | 1.0 | 1.57 | 1.52 | 1.59 | 1.54 |

# Microlens under Melt in-Line Monitoring based on application of Neural Network Automatic Defect Classifcation.

Julien Ducoté [a], Amine Lakcher [a], Laurent Bidault [b], Antoine-Regis Philipot [a], Bertrand Le-Gratiet [a]
[a] STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France
[b] STMicroelectronics, 190 avenue Célestin Coq, 13106 Rousset Cedex, France

The usage of convolutional neural networks (CNN) on images is spreading into various topics in lot of industries. Today in the semiconductor industry CNN are used to perform Automatic Defect Classification (ADC) on SEM review images in almost real time and with level of success as high as trained operators can do or more [1,2]. The possibilities to get new kind of information from images offer to engineers multiple potential usages. In this paper we propose to present derivatives usages of CNN applied to the CD-SEM metrology with specific focus on an application to detect undermelted microlens in our imager process flow [3].

CD-SEM metrology is used to perform Critical Dimension (CD) measurement on almost all patterning steps in the wafer cycle (after lithography and after etch). CNN allows us to get more information from pictures than only dimensions measured by the CD-SEM used to feed a control card.

In our imager process flow we have steps to form microlenses. The microlens process fabrication consists in a first lithography step where microlens matrix is defined in resist. The result is a matrix of quite square parallelepipoid microlenses followed by a melting step in order to reflow resists and eventually form microlens with spherical cap shape. The figure 1 shows the evolution of microlens shape in function of melting process time.

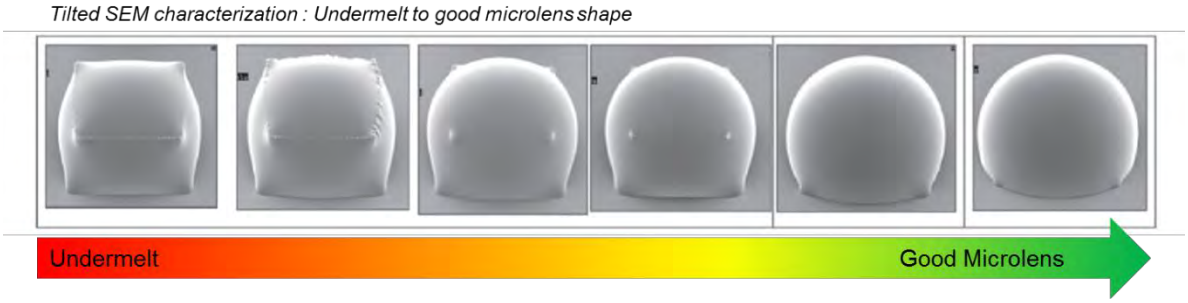


*Figure 1: Melting process on microlens, pictures on left are undermelted microlens, and pictures on the rights are microlens with good shape.*

The microlens melting step is controlled by a CD-SEM measurement that monitors the gap between two microlenses. The figure 2 shows typical images recorded on CD-SEM covering a range from undermelted microlenses to well-formed microlenses.

In all cases showed in figure 2 the gap measurement is within process specifications, meaning that no warning will be sent to fab automation system and the lot will continue to the next process steps. This is not suitable because such undermelted microlenses causes bad light focusing onto the below photodiodes and results in a poor quantum efficiency.


*Figure 2: CD-SEM images of melting process on microlens, pictures on left are undermelted microlens, and pictures on the rights are microlens with good shape. For all images the in-line gap measurement is in specifications.*

There the Automatic Defect Classification seems to be a relevant solution to detect microlenses with bad shape (i.e. undermelted microlenses). Indeed the CD-SEM pictures look similar but the

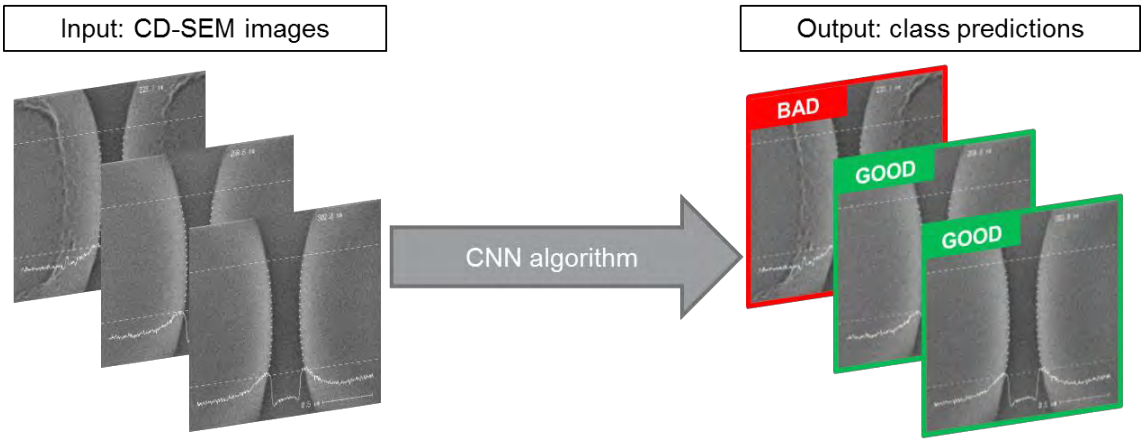


*Figure 3: Convolutional neural network based defect detection applied on microlens CD-SEM images. The CNN returns a prediction ("good" or" bad") for each image.*

undermelted microlenses show significant edge roughness close to the resist top. There a convolutional neural network can be trained to classify pictures in two classes: "good" for microlenses with correct shape, and "bad" for undermelted microlenses. A set of CD-SEM images considered "good" and a set considered "bad" are generated. The "good" set is taken from production data and the "bad" one is generated by undermelting a wafer. Those data sets has been used to train a specific model. The figure 3 illustrates the automatic defect classification based on CNN applied on CD-SEM images of microlenses.

With the appropriated IT structure we are able to get in quite real-time (with a minute) the classification result at the CD-SEM metrology step. Thus a classification "good" or "bad" is associated to each CD-SEM picture. The next step is to send feedback immediately after classification to the fab automation system in order to stop lots with "bad" microlenses (and then send them back to lithography step to rework process).

We are currently optimizing the CNN algorithm to get sensibility aligned with the human eye detection capability. The goal is to be sure that images flagged as "bad" are really undermelted cases and that no undermelted microlenses are flagged as "good". This algorithm improvement is performed through ADC prediction review and with manual classification to create new sets of data when needed. Classified images can be used to create new sets, especially if the classification failed to attribute the correct class (in this case the image is reattribute to the correct set).

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# Machine Learning applications in overlay prediction

**Auguste LAM**

STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France

**ABSTRACT**

The extreme miniaturization of Integrated circuits is causing an unprecedented increase in the manufacturing complexity from node to node. The number of process steps is growing steadily. Each process can be very sensitive to subtle environmental and machinery variations. Overall, the increase of production process steps results in a higher risk of yield loss. Consequently it is a greater and greater challenge to bring a process to maturity leading to an increasing time for product commercialization. Similarly, when a production tool becomes instable, it produces issues along the whole production line. These problems should be addressed very quickly, to guarantee a sustained quality. However, the identification is not an easy task. Big Data Analytics and Machine Learning can be beneficial to operations and maintenance by providing opportunities such as

- Predict upcoming issues in a system or equipment and enable proactive corrective actions
- Correlate failures with critical parameters
- Get faster root cause identification
- Prevent quality excursion

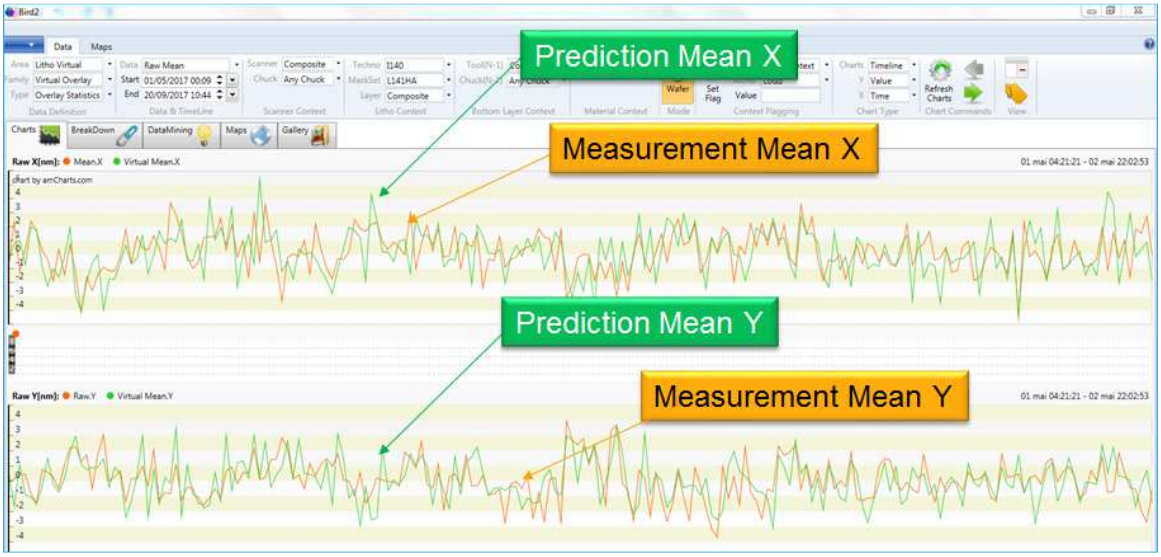
Research in Big Data Analytics at ST focus on developing algorithms, workflows and tools to convert massive volumes of unstructured data into meaningful information in terms of process and equipment knowledge. In ST Crolles300 Fab, Data Analytics are being tested to predict overlay results and detect excursions. The approach is based on a combination of Machine Learning models and Engineering models. Information contained in volumes of data and guidance provided by domain expertise are used together to deliver robust and reliable predictions.

As shown in Table 1, Insertion of knowledge in learning network can be formalized using different approaches depending on available information.

| | Quantitative knowledge *(Equations & Maths)* | Qualitative knowledge *(Gross behavior)* | No knowledge |
|---|---|---|---|
| Contextes | ✓ | ✓ | ✗ |
| Interactions | ✓ | ✓ | ✗ |
| Physical Model | ✓ | ✗ | ✗ |
| | Causal Network | Bayesian Belief Networks | 'Brute Force' Machine Learning |

Table1: Knowledge level can vary from fully described behavior to absolutely unknown mechanisms.

A Machine Learning (ML) model powered by an inference engine is used at ST Crolles for Overlay prediction. A demonstrator software has been developed to evaluate the prediction performances. The early results are promising: prediction errors are less than a few nanometers (Graph 1 for Overlay Mean X & Y).




Graph1: Comparison of Predicted vs Measured Overlay Mean X & Y using Machine Learning

Optimizations on the ML model to further improve the prediction capability are being carried-out.

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Dr. Ronald Schnabel
Stresemannallee 15
D-60596 Frankfurt am Main Phone: ++49-(0)69-6308-227
Fax: ++49-(0)69-6308-9828
E-Mail gmm@vde.com

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